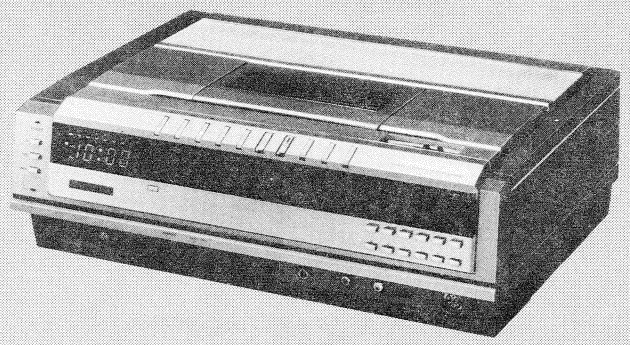
**SERVICE DATA**
**FILE NO. 033-021**

# CIRCUIT AND MECHANICAL DESCRIPTION

# TOSHIBA

## COLOR VIDEO CASSETTE RECORDER

# V-8000T/C/U



## SPECIFICATIONS

| | |
|---|---|
| **General** | |
| Video recording system: | Rotary two head helical scanning |
| Video signal: | EIA standard NTSC color |
| Storage temperature: | −20°C to +60°C (−4°F to +140°F) |
| Operating temperature: | 5°C to 40°C (41°F to 104°F) |
| Antenna: | 75-ohms external antenna terminal for VHF<br>300-ohms external antenna terminal for UHF |
| Channel coverage: | VHF channels 2−13<br>UHF channels 14−83 |
| VHF output signal: | Channel 3 of 4 (selectable)<br>75-ohms unbalanced |
| Power consumption: | 54W |
| Weight: | 13.5kg |
| Dimensions: | 465 x 153 x 360mm (W/H/D)<br>(18.3 x 6.02 x 14.17 inches) (W/H/D) |
| **Video** | |
| Input: | VIDEO LINE IN:<br>Phono-type connector<br>1.0V(p-p) +1.0V (p-p) −0.5V (p-p)<br>75-ohms unbalanced, sync. negative |
| Output: | VIDEO LINE OUT:<br>Phono-type connector<br>1.0V (p-p) ± 0.1V (p-p), 75-ohms unbalanced, sync. negative |
| Signal to noise ratio: | Better than 45dB |

| | |
|---|---|
| **Audio** | |
| Input: | AUDIO LINE IN:<br>Phono-type, 68k-ohms, −10dB<br>MIC:<br>Mic jack (φ6), −70dB<br>suitable for microphone with more than 680-ohms impedance |
| Output: | AUDIO LINE OUT:<br>Phono-type, less than 10k-ohms, −5dB, unbalanced<br>(load: more than 50k-ohms) |
| Frequency response: | 50Hz to 8,000Hz |
| Signal to noise ratio: | Better than 40dB |
| Audio distortion: | Less than 4% at 400Hz |
| **Tape transport** | |
| Tape speed: | SP 20mm/sec., LP 13.3mm/sec. |
| Maximum recording time: | 300 min. with Toshiba L-830 tape (LP mode) |
| Fast forward time: | Within 3.5 min. (L-500) |
| Rewind time: | Within 3.5 min. (L-500) |
| **TIMER** | |
| | LED digital display<br>Count down from AC line frequency. |

Design and specifications are subject to change without notice.

**Caution:** The unauthorized recording of television programmes and other materials may infringe on the rights of others.

# SECTION 1 ELECTRICAL CIRCUIT DESCRIPTION

## 1-1. VIDEO SYSTEM (PW2232)

### 1-1-1. General

The V-8000's Video Circuit built on PW2232 is made more compact than those of the previous VCR with use of newly-developed, highly-dense ICs. It contains a recording and playback amplifiers, a Y comb filter noise canceler, and other functional circuits.

The ICs Used and their applications and functions are tabulated below.

| NAME | APPLICATION | FUNCTIONS |
|---|---|---|
| TA 7636P (30 pins) | Y playback | FM demodulation, non-linear de-emphasis, noise canceler, Y-C mixing, and muting. |
| TA7637P (30 pins) | Y recording | AGC, sync separation, sync tip clamping, non-linear pre-emphasis, dark clipping, white clipping, DC compensation, and FM modulation. |
| CX-188 (24 pins) | Color conversion | ACC, ACK (automatic color killing), frequency conversion, 3.58 MHz crystal-controlled oscillation, and APC detection. |
| CX-196 (24 pins) | Color synchronization | Horizontal sync separation, 175 $f_H$VCO, AFC/APC, $1^2$L counter, mislock detection, frequency conversion, and carrier phase inversion switcher. |
| CX-134 (24 pins) | Preamplifier | RF playback amplification RF switching, and dropout compensation. |
| CX-135 | Y comb filter noise canceler | FM demodulation, limiting, and addition. |

The Video Circuit, a block diagram for which is shown in Fig. 1-1, will be briefly described in this and following paragraphs. The composite video signal input to the Video Circuit is fed to the AGC circuit and color circuit. The AGC circuit uses the NTSC composite video signal itself for AGC action. A part of the AGC output signal is fed as the E-E video signal to the video line output terminal and RF modulator. The E-E signal, also, is fed to the vertical sync separator in the Servo Circuit board, PW2233, for use as the reference signal to the Servo Control Circuit.

On the other hand, the other part of the AGC output signal has the C (chroma) signal component eliminated througth the comb filter circuit. The result is that the Y (luminance) signal component is obtained. The Y signal passes the non-linear pre-emphasis circuit and is converted to FM Y signal by the FM modulator. The FM Y signal is fed to the recording amplifier circuit.

In the color circuit, the composite video signal passes through the 3.58 MHz band-pass filter to separate the C signal. The gain of C signal is controlled to a required amplitude by the ACC circuit. It, then, is frequency-converted to 688 kHz, which is fed to the recording amplifier circuit. The recording amplifier circuit superimposes the 688 kHz converted low-frequency C signal and FM Y signal. The superimposed video signal is connected to the pair of video heads.

In playback, the video signal picked up by the pair of video heads is amplified through the playback amplifier. The FM Y signal of the video signal passes the DOC (dropout compensator) circuit, enters the Y comb filter noise canceler, and then comes into the non-linear de-emphasis circuit where the original Y signal is obtained. The 688 kHz low-frequency C signal, on the other hand, is frequency-converted to 3.58 MHz. The signal and 3.58 MHz C signal are mixed to playback the original NTSC composite video signal.

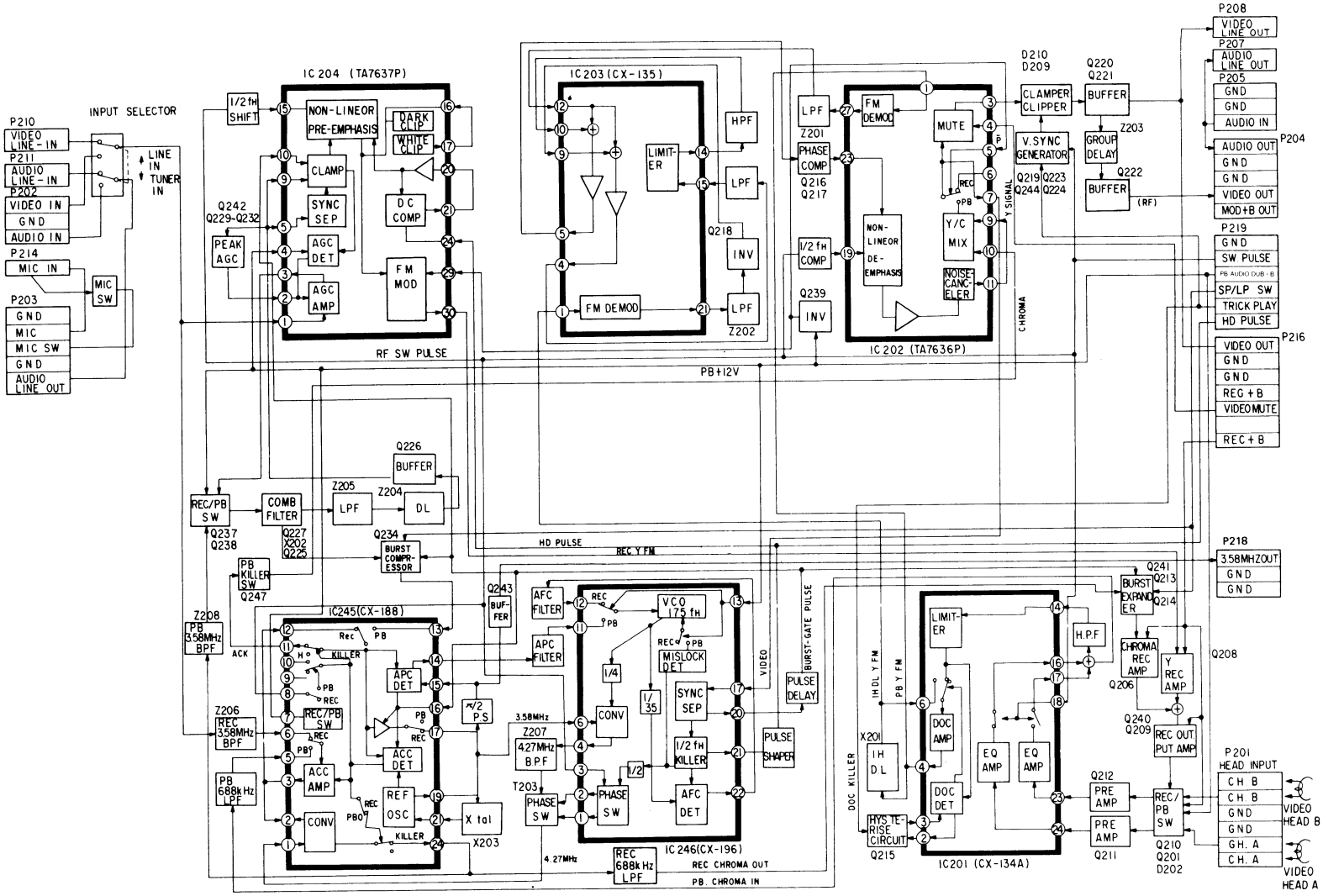



**Fig. 1-1. Video Circuit Block Diagram, PW2232.**

### 1-1-2. Recording-Playback Method of V-8000

The previous Toshiba's β-format VCRs that employ an oblique azimuth, high-density recording system were capable of recording or playback as long as two hours with use of a small sized cassette tape. The present V-8000, like the preceding V-5425, is further increased in the recording density, available in an additional βIII format where three-hours recording can be made using the L-500 cassette as well as in the usual βII. The track pitch of the βIII format is 19.47 μm, the head width 27 μm, and tape speed 13.3 mm/sec, while those of the βII format for the V-5530 are 29.2 μm, 36 μm, and 20 mm/sec. These are tabulated below.

Table 1-1 Major Characteristics of βII and βIII Formats for V-8000 with those of Previous Models for Comparison.

| Model | V-8000 (Present) | | V-5530 (Previous) |
|---|---|---|---|
| Format | βII | βIII | βII |
| Track pitch (μm) | 29.2 | 19.47 | 29.2 |
| Head width (μm) | 27 | 27 | 36 |
| Tape speed (mm/sec) | 20 | 13.3 | 20 |
| Relative speed (m/sec) | 6.993 | 6.999 | 6.993 |

Outstanding features of the β Format recording-playback method are briefly explained below.

#### 1-1-2-1. Guard Bandless Recording

The present βIII format achieves the high-density recording in the manner that the guard band provided between adjacent video tracks in the previous models is eliminated as azimuth loss involved between the video heads is used. In such a guard bandless recording, on of the two heads is made to slant +7 degrees and the other -7 degrees. This eliminates the crosstalk caused from the adjacent tracks. This is called the "azimuth effect". The azimuth effect, however, is not highly gained at such a low frequency as of the frequency-converted C signal. For the reason, a new color signal recording (PI color recording system) is used to eliminate the color crosstalk.

#### 1-1-2-2. Short-wave Recording

The diameter of the head drum used is as small as 74.49 mm. This results in that the relative speed between the heads and tape is as low as approximately 7 m/sec, where the maximum recording wavelength is as short as 1.5 μm. To achieve recording of such a short-wave signal. The video head gap is made narrow to 0.55 μm, thereby improving the playback sensitivity of short-wave signal.

#### 1-1-2-3. Narrow Track Recording

The video track width is made as narrow 29.2 μm for the βII format and 19.47 μm for the βIII format to reduce tape consumption. As such a narrow track recording is employed, non-linear emphasis circuit is additionally used to improve the signal-to-noise ratio for the Y signal. The tape speed is 20 mm/sec for the βII format and 13.3 mm/sec for the βIII format. For more information, refer to Section 1-1-3, the "Luminance Signal Processing Circuit".

| Format | βII | βIII |
|---|---|---|
| A = Tape width (mm) | 12.65 | 12.65 |
| B = Video track pitch (μm) | 29.2 | 19.47 |
| C = Video width (mm) | 10.62 | 10.62 |
| D = Control track width (mm) | 0.6 | 0.6 |
| E = Audio track width (mm) | 1.05 | 1.05 |

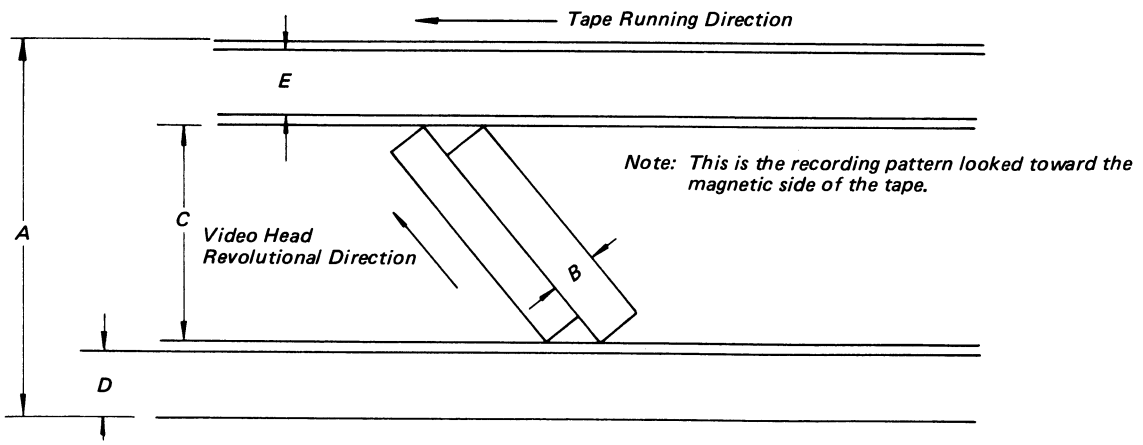



Fig. 1-2 Tape Recording Pattern

### 1-1-2-4. Y Comb Filter Noise Canceler

The Y comb filter noise canceler, which has a comb filter consisting of a 1 H delay line, extracts from the played back FM Y signal only the vertical beat bars due to crosstalk and noise components having no relation to the so-called "1 H shift process" and then adds these in the opposite phase to the original FM Y signal to cancel out them, thereby obtaining improved signal-to-noise ratio.

It is possible for noise canceling arrange such a comb filter that the video signal is derectly delayed by 1 H. However, since the 1 H delay line to be used must be made to have a very wide frequency band, it is not available for the practical use. In the circuit construction employed in the V-8000, a small-sized glass delay line passes the FM Y signal itself. It, also, can be used in common for dropout compensation.

Fig. 1-3 shows a block diagram for the Y comb filter noise canceler circuit. As shown in the figure, the played back FM Y signal is divided into two parts: one is directly demodulated and the other is delayed 1 H before being demodulated. The respective demodulated video signals (termed a "directly demodulated vidio signal" and "1 H delayed, demodulated video signal") are illustrated in Fig. 1-4a and 1-4b. The sine wave on the video signal is an illustrative crosstalk component; and, the video signal is not emphasized for simplicity of illustration.

In recording, the carrier of the FM Y signal in the channel B is shifted fH/2. This means that the 1 H delayed, demodulated video signal (Fig. 1-4b) is shifted 180 degrees from the directly modulated video signal (Fig. 1-4a). The former is subtracted form the latter in the mixer 1 in Fig. 1-3 to obtain the crosstalk component only as in Fig. 1-4c. This crosstalk component is amplitude-halved and then is subtracted from the original signal (Fig. 1-4a) by the mixer 2. The resulting video signal does not have crosstalk component as this was fully canceled out as in Fig. 1-4d. Theoretically, the crosstalk component can be fully canceled out as long as the above-mentioned fH/2 shift is correct, and the random noise is reduced 3 dB. As for video signal of a picture pattern which changes abruptly in the vertical direction and the signal obtained in the way that the signal having no relation to the 1 H shift process around the vertical sync signal is subtracted through the mixer 1, they have considerably high pulsating amplitude as compared with the crosstalk and noise components. Subtraction of the high-amplitude signals from the original demodulated signals results in a vertical resolution decrease or no vertical synchronization. To dissolve such problems, there is provided a limiter that suppresses the high pulses. For the signals left emphasized, they are passed through a lowpass filter (which serves as substantially a de-emphasis network) in advance to allow limiting the crosstalk component as well as noise components. The limited signals are further passed through the high-pass filter (which serves substantially a pre-emphasis network) before subtraction from the original signals.

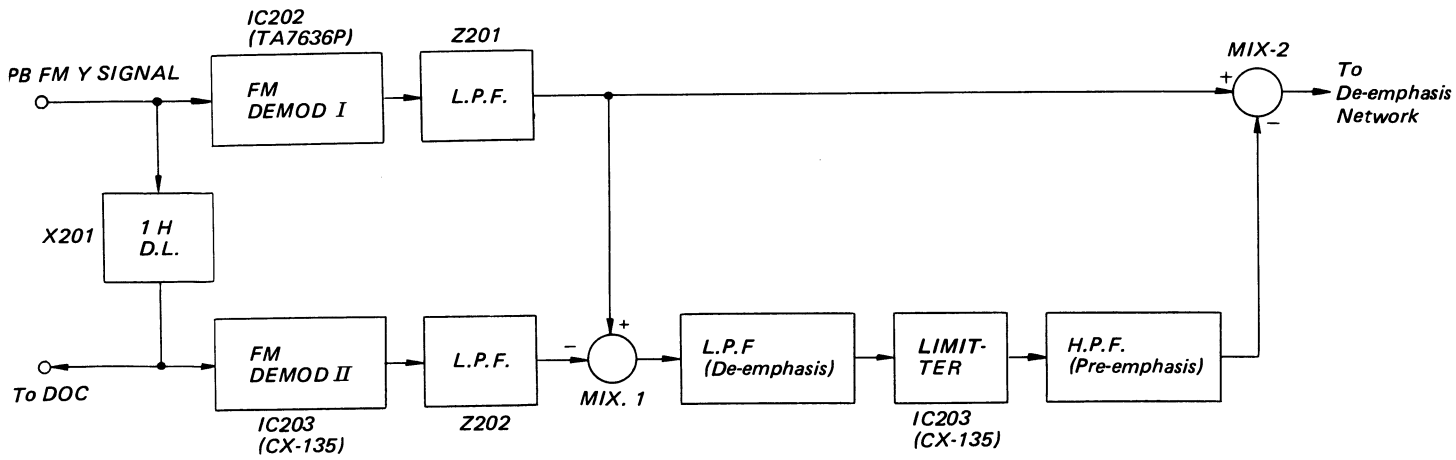



**Fig. 1-3 Y Comb Filter Noise Canceler Circuit Block Diagram.**

a Video Signal which is Demodulated Directly

b Video Signal which is 1 H Delayed and then Demodulated

c Crosstalk Component Obtained by Subtraction in Mixer 1

d Video Signal Obtained by Canceling out Crosstalk Component in Mixer 2

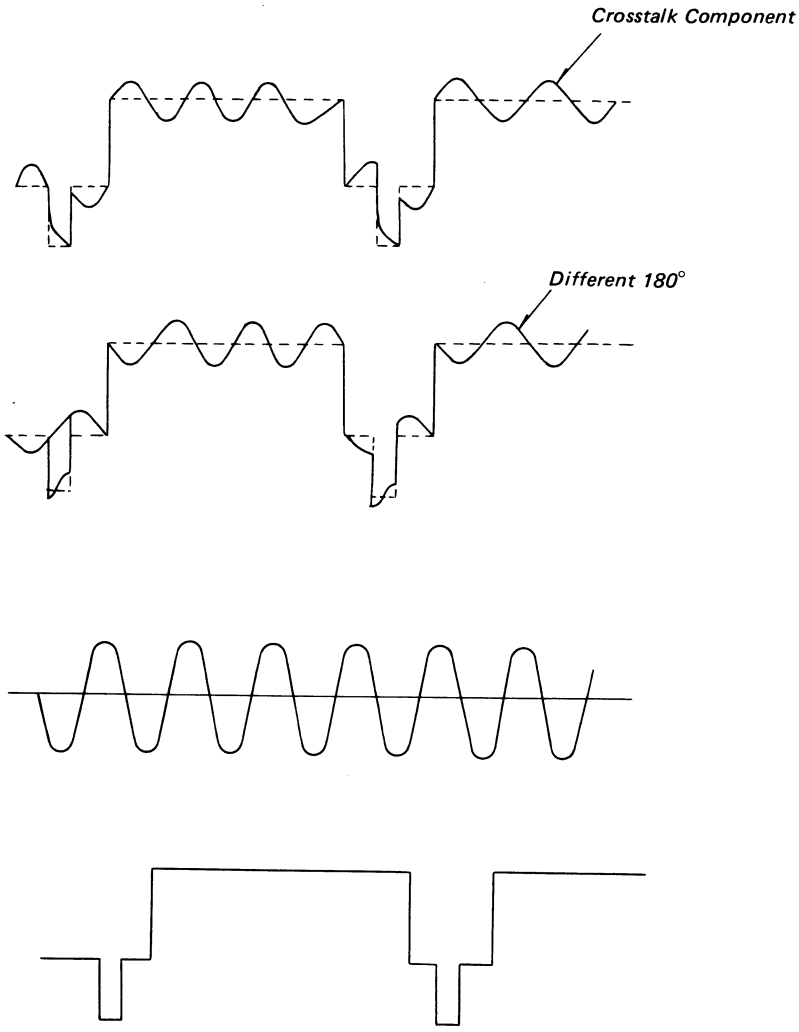



Fig. 1-4 Comb Filter Noise Canceler Circuit Video Signal and Crosstalk Signal

### 1-1-2-5. Color Recording System (PI C Signal Recording Method)

The NTSC Color Recording System used in the V-8000 separates the Y (luminance) and C (chroma) signals are separated, the Y signal of which is frequency-modulated (FM recording) and the C signal is converted to a low frequency and is amplitude-modulated (AM recording) in the same way as the previous recording method. (see Fig. 1-5 below.)

The Y signal frequency deviation by the frequency modulation ranges from 3.6 to 4.8 MHz. The C signal of 688 kHz converted from 3.58 MHz cannot be made free of adjacent channel crosstalk by the azimuth recording method because of low frequency. To avoid the crosstalk in the C signal, the PI (phase invert) color recording method is employed, in which when recorded, the C signal is phase inverted 180 degrees on the track A every horizontal sync interval (1 H) and that on the track B is continuous in the phase as illustrated in Fig. 1-6. The phase inversion is made by inverting the phase of the 4.27 MHz carrier of the converted C signal.

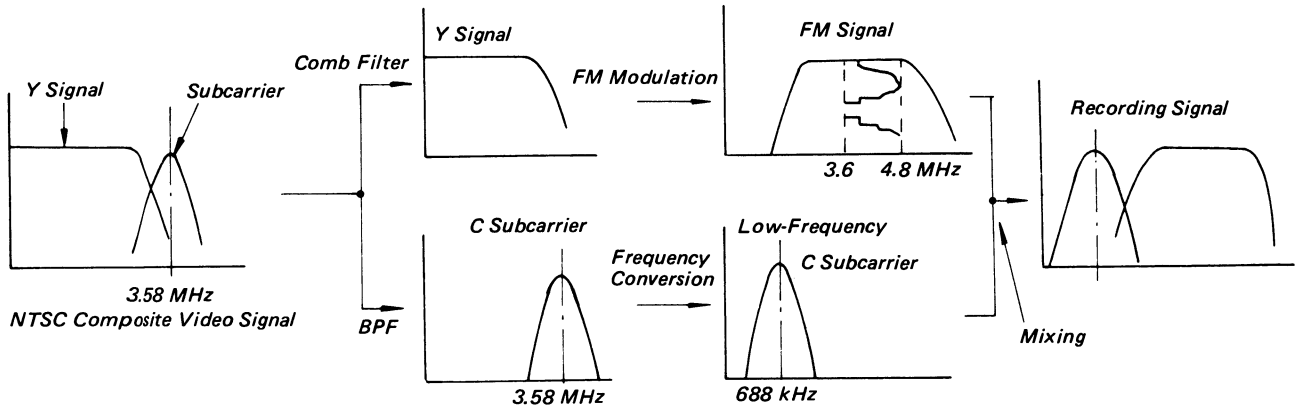



**Fig. 1-5 Recording Signal Frequency Distribution**

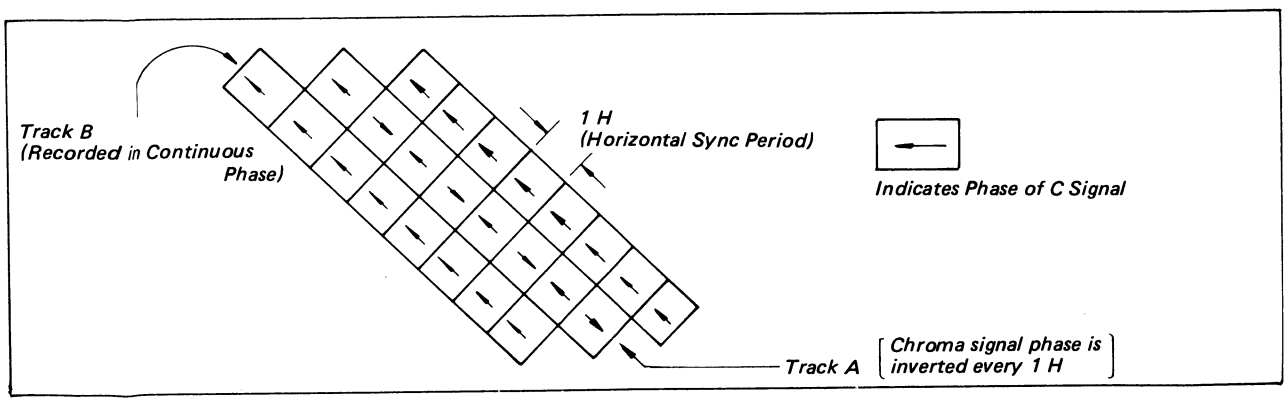



**Fig. 1-6 C Signal Recording Pattern**

The relationship of the played back signals from the recorded tape in the PIC signals recording method is shown in Fig. 1-7.
The playback chroma (C) signal from each track contains the crosstalk picked up of the adjacent track as shown in the dotted arrow in Fig. 1-7 below. The C signal on the track A is phase inverted to recover to the original continuous phase. As a result, the desired playback C signals on the tracks A and B have the same phase relationship with the crosstalk. The two playback C signals are passed through a comb filter, in sequence and is added to the direct playback C signals as shown below. In this process, the crosstalk components on each track cancel out, but the C signal alone is output (see Fig. 1-8).

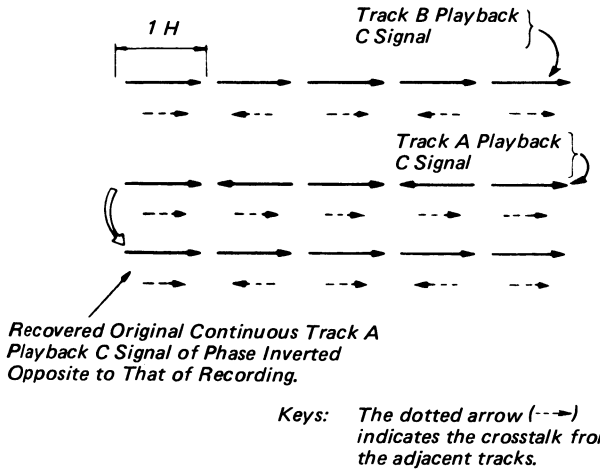



**Fig. 1-7 Relationship Between Playback Chroma Signal and Crosstalk Signal**

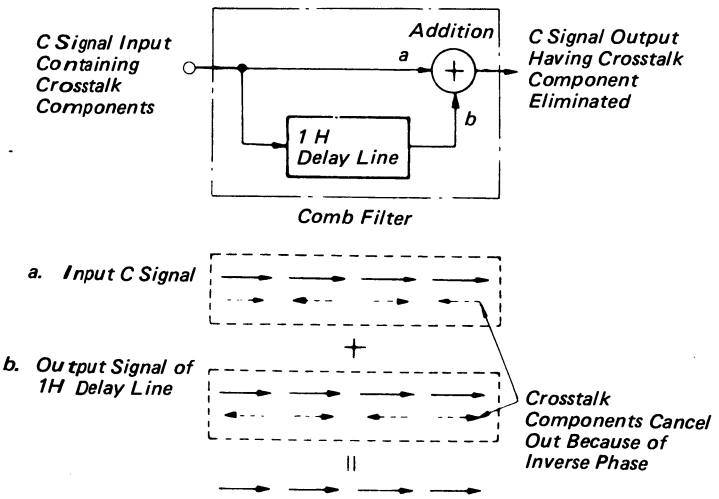
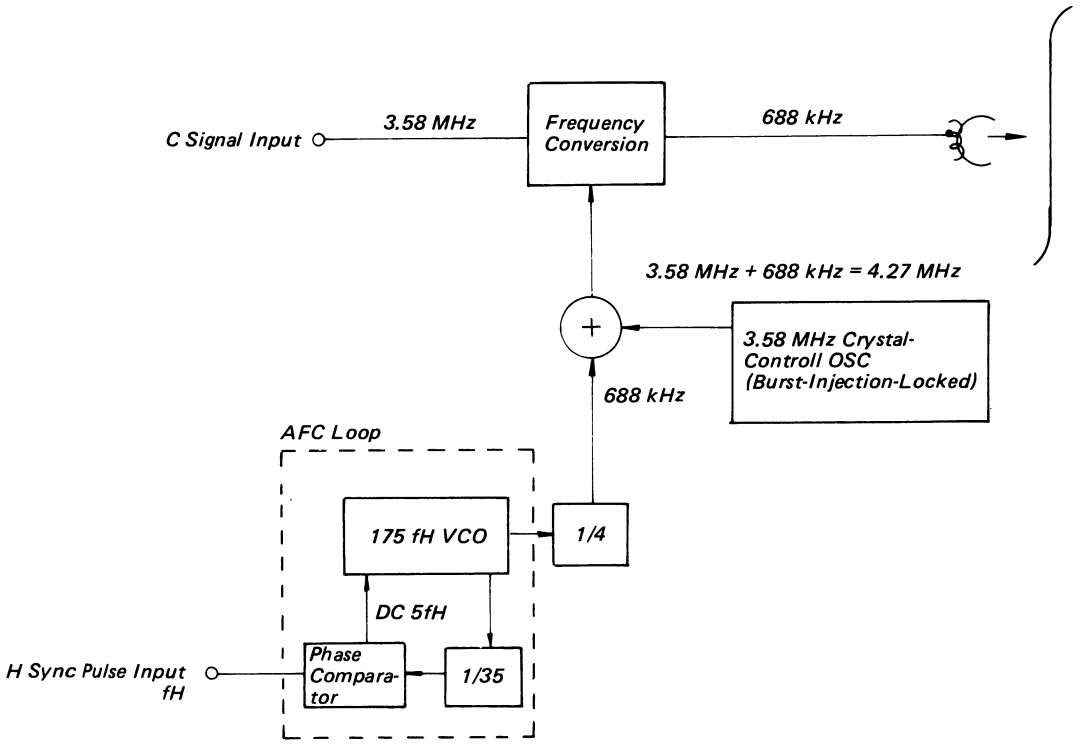
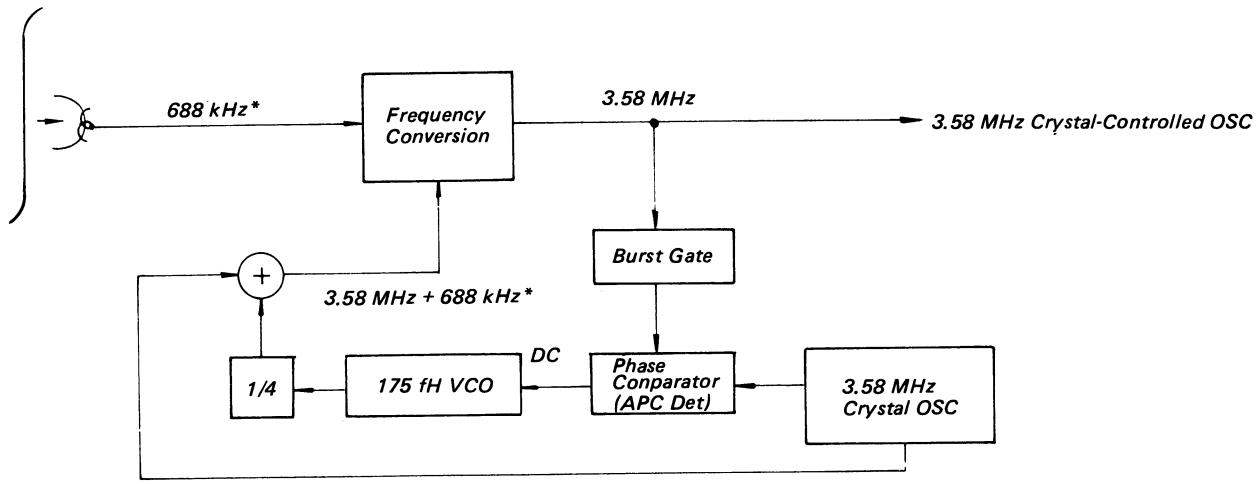



**Fig. 1-8 Elimination of Crosstalk by Comb Filter**

When the signal passed through the 1 H delay line and the direct signal are mixed as shown in Fig. 1-8, the signal components are added because of the same phase, but the crosstalk components are subtracted to eliminate because they are phase inverted every H interval.
The C signal phase fluctuation due to jitters and the like in the recording and playback modes of operation is eliminated by a new APC and AFC circuits including a $I^2L$ digital network in and IC. As seen from Fig. 1-9, the 175 fH VCO (voltage controlled oscillator) produces a signal of 175 fH (= 4 x (44 - 1/4) fH) as high as 175 times the horizontal sync signal frequency, fH. The signal is 1/4 counted down to 688 kHz (= (44 - 1/4) fH). This is added to, the 3.58 MHz signal output of the 3.58 MHz crystal-controlled oscillator which is burst-injection-locked by the burst signal, to produce a 4.27 MHz carrier for low-frequency conversion. The 175 fH VCO signal, on the other hand, is counted down to 1/35 to phase-compare with the horizontal sync frequency fH. The error voltage controls the VCO to correct the frequency. This frequency control loop as call the "AFC loop". The C signal and Y-FM signal are recorded in the above-mentioned frequency relationship.
In playback, the APC loop controls the VCO to cancel out possible phase fluctuation of the C signal. The APC loop shown in Fig. 1-10 compares the phase of the burst signal with the phase of the reference signal of the 3.58 MHz crystal-controlled oscillator, which is a free running oscillator, but not burst-injection-locked oscillator. The error voltage controls the VCO. The present color recording system could be involved in a side-lock phenomenon of the C signal as the VCO frequency range is very wide. To prevent it, additional mislocking detector circuit which enables the system to quickly respond to possible disturbance is provided, thereby providing stable C signal.




**(Recording Mode of Operation)**




*Note: Each of the signals marked (*) contains phase fluctuation.*

**Fig. 1-9 AFC and APC Loops (Playback Mode of Operation)**

### 1-1-3. Luminance Signal Processing Circuits

The luminance (Y) signal processing circuits uses one IC (TA7637P) for the Y signal recording circuit and three ICs (CX-134A, CX-135A, TA7636P) for the Y signal playback circuit. TA7637P contains an AGC circuit, a sync tip clamper, a sync separator, a non-linear pre-emphasis circuit, a white clipper, a dark clipper, a frequency modulator, and a DC compensator. CX-134A contains a playback pre-amplifier, a RF switcher, a limiter, and a dropout compensator. CX-135A contains a frequency demodulator, an adder, and a limiter. TA7636P contains a frequency demodulator, a non-linear de-emphasis circuit, a noise canceler, a Y-C mixer, and a muting circuit.

#### 1-1-3-1. Luminance Signal Recording Circuit

**(1) Video input circuit**

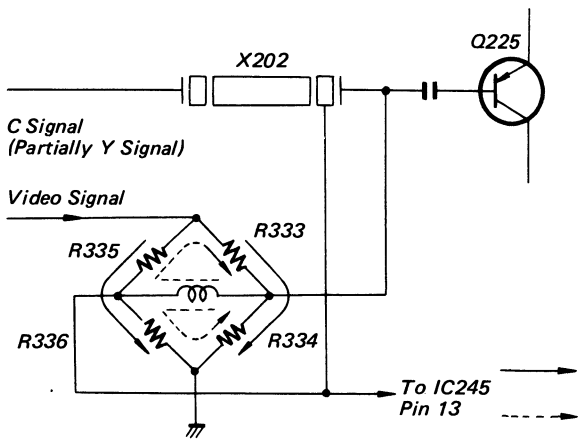
The RF TV signal fed to the V-8000 is demodulated to video signal through the Tuner Block. The video signal is connected to pin-1 on P202, and then to the INPUT SELECT switch S201. The external video signal from a TV camera enters the VIDEO pin jack P210 and also is connected to the same INPUT SELECT switch S201. Either of the video signals is selected by the INPUT SELECT switch. The selected video signal is fed through Z206 to obtain chroma signal and through R329 to the AGC circuit as well.

**(2) AGC circuit, IC204**

Pin-1 on IC204 has the video signal input to the AGC circuit. The AGC circuit controls the constant gain of the video signal in the amplitude and feeds it out from pin-3 on IC204. The signal output of the AGC circuit is fed to the E-E output through pin-6 on IC202 and through the comb filter to the color circuit. Note that the V-8000 has the color circuit only, while the previous model such as V-5425 contained a monochrome circuit and color-monochrome mode switching circuit.

The AGC circuit output video signal fed to the color circuit passes the record-playback switching circuit of Q238 and is branched into two paths: one is amplified through Q227 and passes the comb filter to the matrix circuit, and the other is directly connected to the matrix circuit. At the base of Q225, the two Y signals are added in phase, but the two C signals are canceled out in opposite phase. The 1 H delay line has a band-width of 3.58 MHz ± 0.6 MHz at -3 dB. The result is that the added Y signal is raised up in the frequency response. The frequency response is necessarily compensated for flat to the base of Q226 by C290, L220, and Z205. The Y signal having the C signal eliminated through the comb filter is fed through Q226 to the sync pulse separator in IC204 and to the sync tip clamper.

The Y signal passing the clamping capacitor C299 to pin-9 on IC204 (TA7637P) is sync-tip-clamped by the horizontal sync pulse fed from the sync pulse separator. The clamped Y signal is fed to the AGC detector to restrict the AGC circuit output to a certain level. The clamped Y signal, also, is fed to frequency modulator through the non-linear pre-emphasis circuit.




*Keys: The solid line ( — ) indicates the direct video signal and the dotted line (.....) the video signal passing the 1 H delay line.*

**Fig. 1-10 Y Signal Matrices**

The AGC circuit is used of sync, AGC type. The standard ratio of the video signal level to the sync pulse level (V/S ratio) for the 100% composite video signal is 10 to 4, or 0.714 Vp-p to 0.286 Vp-p for 1 Vp-p composite video signal. The video signal level, however, may change with the brightness of the taken picture. The present sync AGC detects the sync pulse level to make this constant irrespective of any change of the picture brightness. This is accomplished in the manner that as shown in Fig. 1-11, the burst gate pulse is subtracted from the horizontal sync pulse of the sync-tip-clamped video signal at the back porch, and the subtracted horizontal sync pulse is peak-detected. Though the peak detection is made at the pedestal level as shown in Fig. 1-11, it can be said that the amplitude of the sync pulse is detected, as the sync tip level if held constant by the sync tip clamper and the amplitude of the subtracting pulse is constant. Note that for a particularly high video signal component, a different peak AGC detector is provided, which holds the peak-to-peak value of the video signal to a constant level. In fact, R356 is provided for the peak AGC detector so that this may function for 105% or higher video signal input.

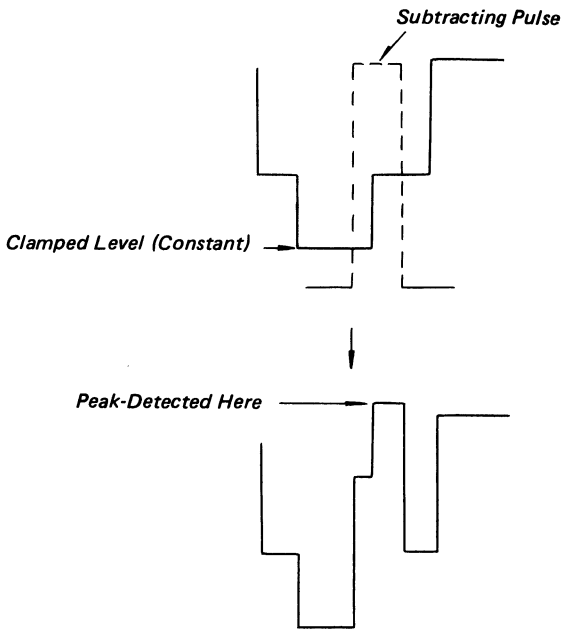



**Fig. 1-11 Sync AGC**

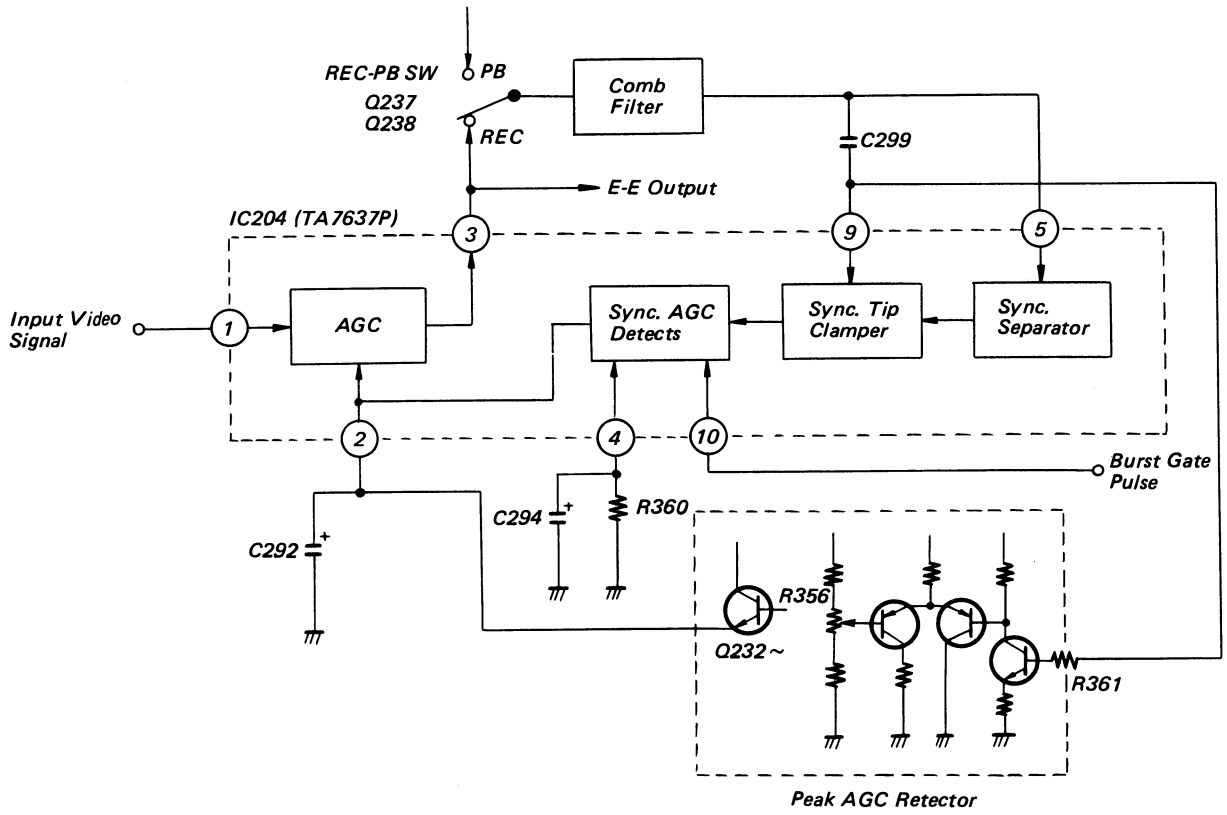



**Fig. 1-12 AGC Circuit (TA7637P)**

**(3) Non-linear pre-emphasis circuit and frequency modulator, IC204**

A block diagram of the frequency modulator and the non-linear pre-emphasis characteristic are shown in Figs. 1-13 and 1-14. The Y signal that has been sync-tip-clamped fed to the non-linear pre-emphasis circuit. In general, the frequency modulator is specified in the frequency deviation. The modulation index is small as the modulation frequency is high, resulting in decrease of the signal-to-noise ratio. To improve this, the response at high frequencies is pre-emphasized in recording.

The sync-tip-clamped signal is highly emphasized at pin-11 on IC204. To prevent such a high emphasis from causing over-modulation, the compressor circuit, consisting of R377, C302, D214, D215, and R362 at pin-12, compresses the signal so high as it was emphasized higher, R378, R379, and C303 at pin-13, further, emphasizes the signal a little and L221, R381, and C304 at pin-15 emphasizes the signal around 2 MHz.

The signal emphasized at high frequencies is clipped out at the level higher than necessary by the dark clipper and white clipper at pins 16 and 17 and is fed to the frequency modulator. The frequency modulator is astable multivibrator type, which oscillates at a frequency determined in terms of the current flowing from pin-26 to R397 and C312, R453 and Q233 adjusts the current to set the FM carrier frequency.

In the guard bandless recording system in the V-8000, the video heads of 27$\mu$m width traces over the track of 29.2$\mu$m width for the $\beta$II format or 19.47$\mu$m for the $\beta$III format in the playback mode of operation. This causes crosstalk, or beat that is a difference between the FM frequencies, of the adjacent tracks. The beat will appear as vertical bars on the TV screen, deteriorating picture quality. To minimize the effect of the beat, the vertical bars are transformed to oblique crosshatch which does not relatively affect the picture quality in the manner that the FM carrier is shifted fH/2 every vertical sync pulse interval (1 V) to interleave. For interleaving, the head switching pulse fed as the field switching signal from the Servo Control Circuit is attenuated in the level by R384, R449, and R357. The attenuated signal is applied to R382 at pin-15 to change the DC bias so that the fH/2 frequency can be varied. The switching pulse level is low in the field A (head A) and high in the field B (head B). The FM carrier frequency in the field B is fH/2 higher than that of the field A. The FM output signal is converted to a low impedance through the emitter follower and then is fed out from pin-30. The low-impedance FM output signal has the components of the frequency band corresponding to the 688 kHz chroma signal eliminated through the trap, consisting of R206, C203, L201, and R205. The resulting FM signal is mixed with the 688 kHz recording chroma signal at the collector of Q208.

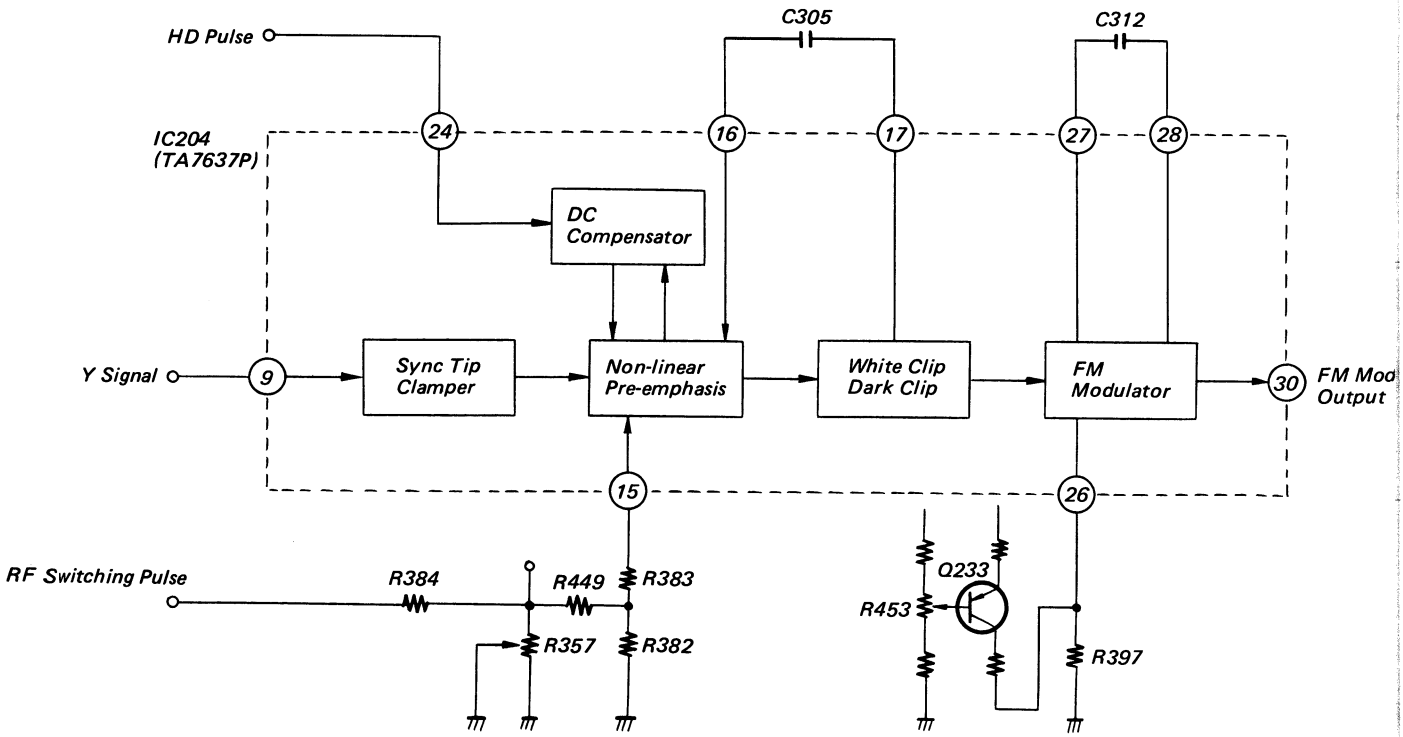



**Fig. 1-13 FM Demodulator Block Diagram**

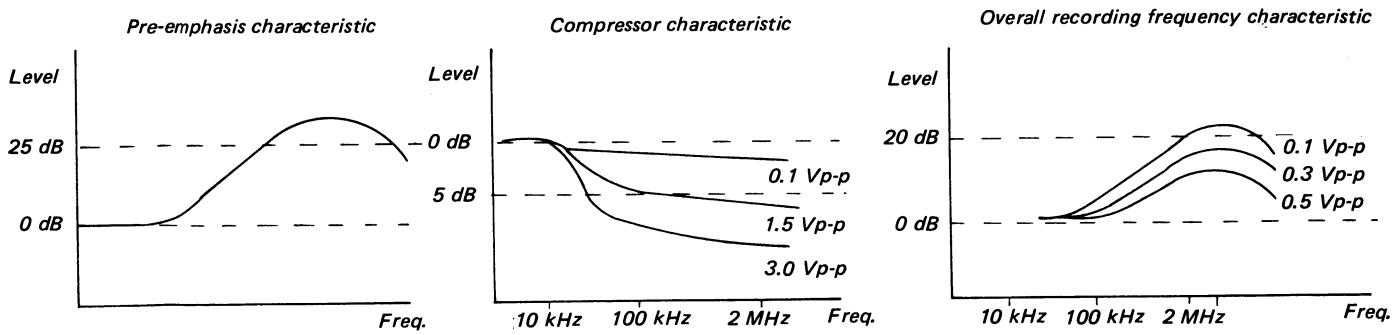



**Fig. 1-14 Non-linear Emphasis Charactristics**

**(4) DC compensator, IC204**

The video signal transmitted from a broadcasting station may change in the DC level every horizontal sync interval as shown in Fig. 1-15 if closely observed. Such a DC level fluctuation disturbs the 1/2 fH interleaving. The result is that the picture quality is deteriorated. To avoid this, the average level of the video signal in each H period is sampled as in Fig. 1-15-b, the difference of the average levels is amplified and phase-inverted as in (C), and this is added to the original signal, thereby canceling out the DC level fluctuation. The HD pulse is frequency-divided through a 1/2 flip-flop for use as the sampling pulse. The average level of the video signal is obtained through the integrator circuit, consisting of C308, C309, C310, R389, and R390 connected to pins 22 and 23 on IC204.

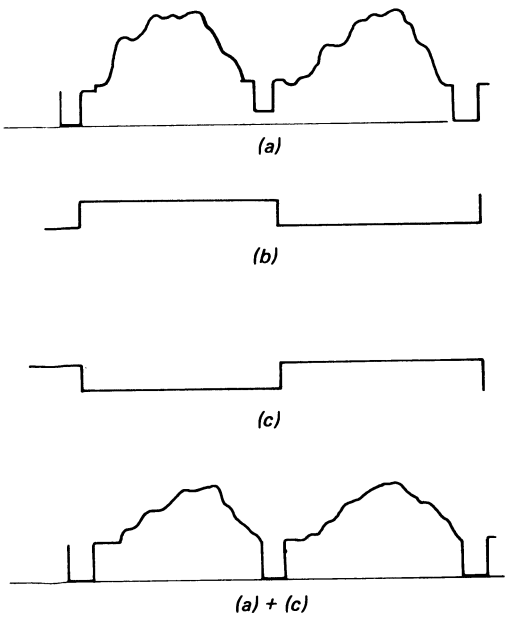



**Fig. 1-15 DC Compensation**

**(5) Recording amplifier**

The 688 kHz chroma C signal, as described previously, is fed from pin-24 on CX-188 through the lowpass filter, consisting of C362, L226, and C363, which serves also for differentially compensating the pair of video heads by 6 dB/oct. The C signal, then, passes the chroma signal recording current level variable resistor R251. It, also, passes the burst expander, consisting of Q206. The C signal, now, is superimposed on the collector of Q210 with the frequency-modulated luminance (FM Y) signal from which the C signal was eliminated, or separated, through the 688 kHz trap. The resulting signal is the original video signal.

The video signal passes the buffer, consisting of Q240. It, also, passes the output amplifier, consisting of Q209. It, further, is delivered through the transformers T201 and T202 and through pins 5 and 6 on P201 and pins 1 and 2 to the pair of video heads A and B, respectively. Although the C signal is recorded in the AM fashion, the FM Y signal functioning equally as the high-frequency bias in audio tape recorders provides a high signal-to-noise ratio sufficiently for recording and playback.

In recording, the +B line is connected to Q209 in the way that the recording +B voltage makes D201 and D202 conduct.

### 1-1-3-2. Playback Premaplifier Circuits

**(1) Video head record-playback switching circuit, (Q210, D201, D202)**

The video head record-playback switching is made by the recording +B and playback +B voltages. For playback, the playback +B voltage is connected through a resistor to the base of Q210 to turn Q210 on. In playback, also, the recording +B voltage is connected through the peaking coil to the anodes of D201 and D202 and the playback +B voltage is applied through the peaking coil and resistor to their cathodes as the reverse bias to hold them turned off. These diodes allow the video signals from the input transformers T201 and T202 to enter the gates of Q211 and Q212, respectively.

**(2) Preamplifier, Q211, Q212, IC201**

A very small signals picked up by the pair of video heads pass through the rotary transformer and the step-up transformers T202 and T203 to the FET amplifiers Q211 and Q212, respectively. The inductance of each video head and the capacitance of C251 or C252 resonate to compensate the response at high frequencies around 5.1 MHz. Q211 and Q212 are connected to the amplifier in the IC201 to form a cascade amplifier.

**(3) Equalizer, IC201**

The output of the cascade amplifier mentioned above is connected through the emitter follower to the equalizer amplifier. The parallel network of inductor, capacitor, and resistor connected as the collector across pins 20 and 21 on IC201, forms the equalizer resonating around 6.1 MHz.

**(4) RF switching circuit, IC201**

The signal output of above-mentioned equalizer is fed to the RF switching pulse is supplied to pin-18 of IC201. If pin-18 is low, the output of the head A is switched to the signal output pin-20. If pin-18 is high, reversely, the output is switched to the power line pin-22. For the head B route, the switching pulse serves for reverse action. Now, the RF signal having the overlapped part of the both fields eliminated is obtained. The RF signals output of the RF switchers pass the amplifiers and emitter followers to pins 16 and 17. The output signals in the two routes are mixed in the resistor network, consisting of R232 and R233, to form a serial signal. The serial RF signal is fed to the chroma signal playback circuit through the serial resonant trap, consisting of L208 and C216.

The serial resonant trap, resonates at 55 kHz. This prevents the erasing oscillator signal from being induced into the C circuit to produce undesired beats in audio dubbing.

The signal mixed through R227 and R228, on the other hand, passes the highpass filter where the C signal is eliminated. The FM Y signal alone is connected to pin-14. Note that the present V-8000 is in the color mode, whereas the previous models had a color-monochrome mode switching circuit.

**(5) Limiter, IC201**

The playback FM Y signal entering pin-14 on IC201 is fed to the limiter. The limiter restricts the FM Y signal amplitude to eliminate possible change. The signal output of the limiter normally passes the DOC switch, which is described below, to the output amplifier. The output amplifier signal is fed out from pin 4. The signal at pin-4 passes the highpass capacitor C230 to the frequency demodulator input at pin-1 on IC202. It, also, enters the glass 1 H delay line X201. The 1 H delay line has a wide frequency band as it also serves as the Y comb filter 1 H delay line.

**(6) DOC (Dropout Compensator), IC201, Q215, X201**

The FM Y signal passing the 1 H delay line is delayed a single horizontal sync pulse interval (1 H). The delayed a signal is connected through pin-6 to the DOC switch. The output of the limiter is detected as dropout pulse by the DOC detector C228 and R246 at pin 7 comprise a smoothing circuit for the detected dropout pulse. The detected signal is applied to the Schmitt trigger to shape it to proper switching pulse. R257 is used to adjust the sensitivity of the Schimitt trigger, thereby setting optimum dropout compensation sensitivity. The output of the Schmitt trigger is applied to the DOC switch as the switching signal. This activates the DOC switch for the presence of dropout to insert into the dropout line the signal a single H before. Q215 connected to pin-2 is turned on or off by the dropout detection pulse to shorten or open R238 accordingly. This provides a hysteresis characteristic for the DOC switch action level. Note that in the still or cue and review playback, good picture cannot be reproduced unless the DOC is turned off. The DOC is turned forcibly off by applying the special playback signal to the connection of R257 and R242 to raise the DC level at pin-3.

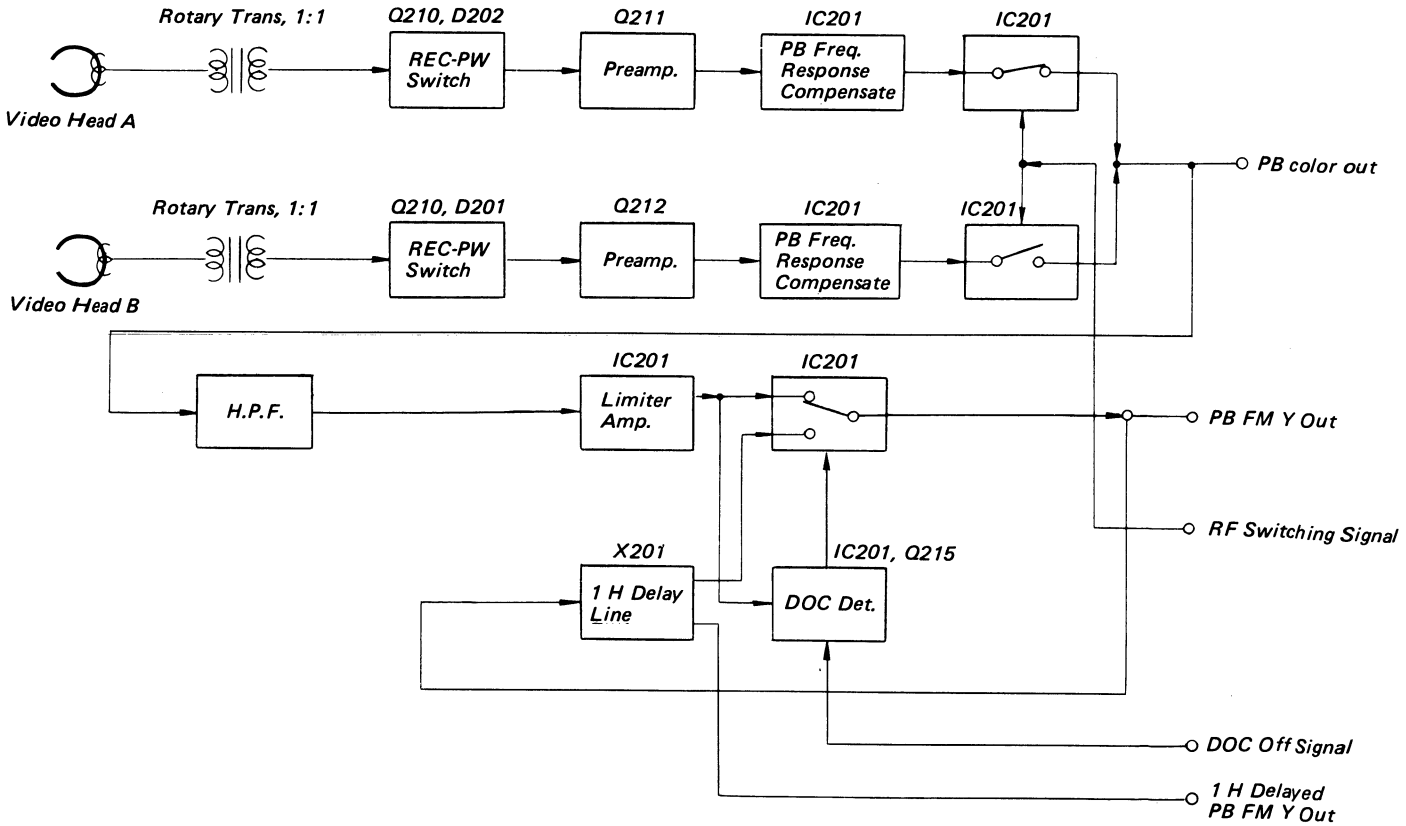



**Fig. 1-16 Playback Pre-amplifier Circuit Block Diagram (PW2232)**

### 1-1-3-3. Luminance Signal Playback Circuit

**(1) FM Y signal demodulator IC202**

To demodulate the FM Y signal, IC202 (TA7636P) has an astable multivibrator-type demodulator. The astable multivibrator in the present FM demodulator is used as a delay line in the manner that the FM signal is injected into the astable multivibrator to lock, making use of the fact that the phase difference between the astable multivibrator output signal and input FM signal is in proportion to the FM signal frequency. The delay time of the injection-locked the astable multivibrator output signal with respect to the input FM signal is constant irrespective of the FM signal frequency. As the delay time is constant, the phase difference of the output signal from the input FM signal is large with the frequency. The phase difference is passed through the phase comparator, or the adder, which produces a demodulated signal in proportion to the input signal frequency. Fig. 1-17 is a block diagram of the FM demodulator.

The FM Y signal passes the highpass filter capacitor C230 to pin-1 on the FM demodulator 1C202. The delay time of the astable multivibrator is determined in terms of the current following from the +10 V line through R248 into pin-28 on IC201. The demodulated signal, applied across the collector load resistor at pin-27, is passed through the lowpass filter Z201 to obtain the Y signal alone.

**(2) Y comb filter noise canceler circuit, IC203, Q218**

The frequency-demodulated signal by IC202 (TA-7636P) passes the lowpass filter Z201, is level-adjusted through R258, and is connected to pin-12 on IC203 (CX135). The 1 H delayed FM Y signal which passed the 1 H delay line X201, on the other hand, is connected to pin-1 on IC203 (CX135). This demodulates the signal to the original Y signal. Note that the FM Y demodulator in CX135 is of the same multivibrator form as that of TA7636P.

The demodulated Y signal is fed out from pin-21 on IC203, passes the lowpass filter, and is phase-inverted through Q218. The Y signal enters pin-9 on IC203 (CX135) through R259.

The noise component having no relation to the 1 H shift process is obtained in a subtraction way. It is output from pin-4 on IC203 (CX135). The crosstalk component is also fed out from pin-4. As these are on the pre-emphasized signal, this is passed through the simplified de-emphasis network, consisting of R297, C267, R298, C268, and R299, together with the noise and crosstalk components. The de-emphasized signal containing the noise and crosstalk components enters the limiter at pin-15 on IC203. The limited signal is passed from pin-14 through the simplified pre-emphasis network, consisting of C265, R296, C264, and R295. The pre-emphasized signal enters pin-10 on IC203 (CX135) and now is subtracted from the main signal coming from pin-12 on IC203 (CX135). In other words, the signal from IC202 (TA7636P) comes from pin-12 on IC203 (CX135) and the crosstalk component from pin-10. The subtracted signal including the noise-canceled video signal and crosstalk component is fed from pin-5 on IC203 (CX135) to the base of Q216 and is delivered to the normal de-emphasis network.

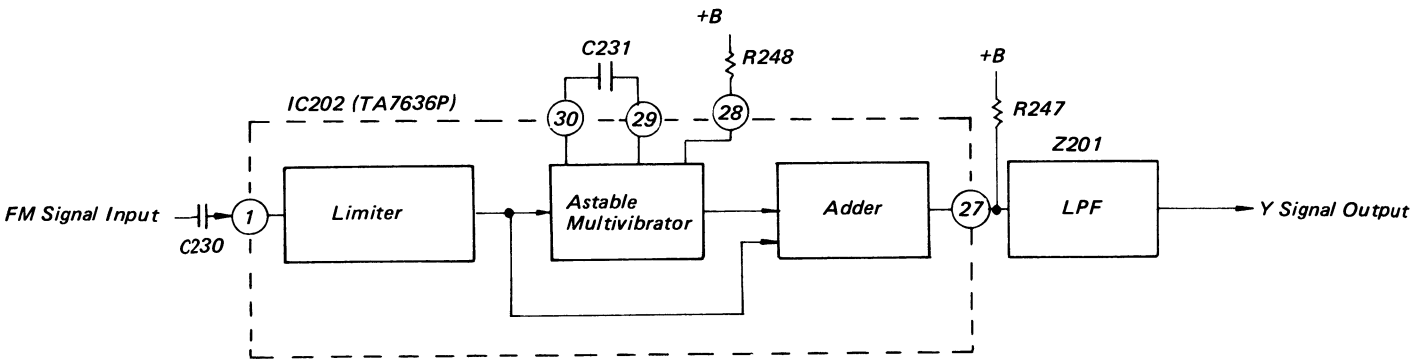



**Fig. 1-17 FM Demodulator Block Diagram**

**(3) Non-linear de-emphasis circuit, IC203**

The Y signal which passed the Y comb filter noise canceler comes from pin-5 on IC203 to the base of Q216. The Y signal is phase-compensated through L214, C234, and R263, and further is smear-compensated through R265, R266, and L215. The Y signal with the carrier attenuated by L216 and C236 is input from pin-23 on IC202 to the non-linear de-emphasis circuit and is expanded by the expander connected to pin-22. The expander consisting of C239, R268, R269, D204, D205, R271, and R272 provides the Y signal with the characteristic contrary to the one that has been obtained by C305 and the white clipper inside IC204.

The expanded Y signal is compensated in the frequency response through R270, L217, and C238 and is de-emphasized through R275, R274, and C241 connected to pin-21 to obtain the characteristic contrary to that of R378, R379, and C303. The RF switching pulse is applied to the cross point between R277 and R278 connected pin-19 through R279. The head switching pulse changes the bias so that the DC level fluctuation occuring every vertical period may be leveled. The fluctuation, as described previously, is due to the demodulation of the FM Y signal carrier-shifted 1/2 fH every vertical period in recording. The Y signal of constant DC level is de-emphasized through L218, C243, and R280 again to the characteristic contrary to the one of L221, C304, and R381. The Y signal further is compensated in the frequency response through C244, L219, and R238 connected to pin-17. The Y signal is expanded through the expander consisting of D206, D207, R284, and C245 again to the characeristic contrary to the one of D214, D215, R362, and C302.

The expander emphasizes the high-level parts of the Y signal together with the above-mentioned expander. Finally, the Y signal is de-emphasized through C246, R285, and R286 connected to pin-16 to the characteristic contrary to the one of C301, R375, and R376, and is connected to the gain control amplifier. The gain control amplifier has R300 and R476 that determine the amount of feedback gain from pin-14 to 15 to provide a final video signal level of 10 Vp-p at 75 Ω terminal.

**(4) Noise canceler, IC202, C271, R301**

A block diagram of the noise canceler is shown in Fig. 1-18. In the figure, the high-pass filter, consisting of C271 and R301, passes the high-frequency component of the Y signal. The high-frequency component is passed through the limiter to eliminate the signal component to obtain the noise component. The noise component is added in opposite phase and same amplitude to the original signal to cancel out.

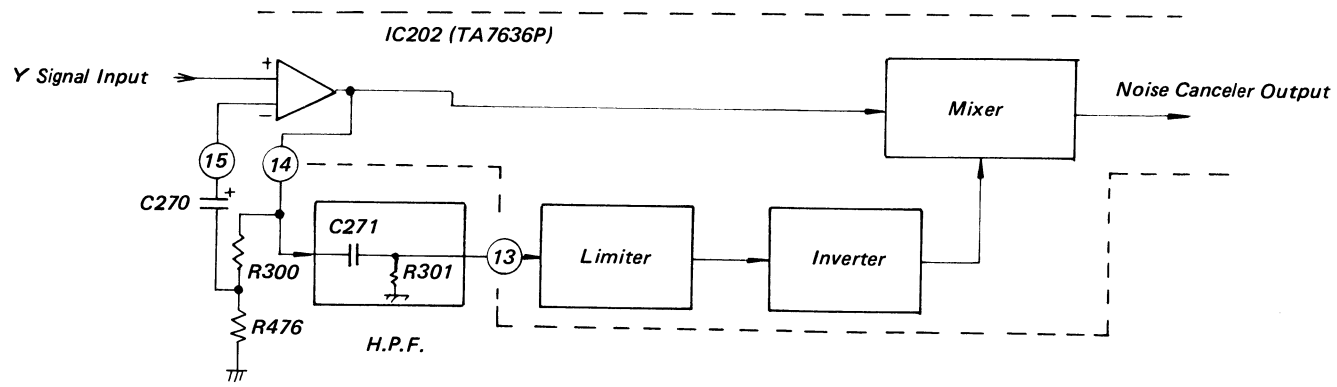



**Fig. 1-18 Noise Canceler Block Diagram**

**(5) Y-C mixer, IC202**

The Y signal output of the noise canceler and the playback C signal input to pin-10 are mixed. The amount of mixing can be adjusted with R351 (ACC). In the color mode, pin-10 is biased to 3.6 V, approximately. When the color killer is activated, however, the color killer signal makes Q247 to conduct to ground pin-10. The result is that the Y-C mixer stops mixing for the monochrome mode.

**(6) EE Record-play video switching circuit, IC202**

The Y-C mixed vidio signal is connected to the record-playback video switching circuit inside IC202. The video switching circuit is controlled by the voltage to which the playback +B voltage is inverted. The signal output of the video switching circuit is fed to the muting circuit inside IC202 and also is fed from pin-7 to the sync separator in IC246 (CX196). In a mode other than the playback mode of operation, the video switching circuit is set to the record position, from which the E-E video signal connected to pin-6 is output. The record-playback video signal having passed the muting circuit is fed out from pin 3.

**(7) Muting circuit, IC202**

The muting signal output form the Logic Circuit board PW2233 is fed through pin-5 on P216 to pin-4 (muting signal input) on IC202 to mute the video signal.

**(8) Clamping and clipping circuit**

The video signal output of pin-3 on IC202 (TA7636P) is soft-clamped at the anode voltage of D208 through R308 and D209. It could occur that the white peak is too high in case, for example, of using a video camera, as compared with the usual one. The excessive video input signal overmodulates the RF modulator, resulting in buzz in the sound. To dissolve such a problem, the excessive video input signal is clipped by D210 in reference to the voltage at the connection of R308 and R307.

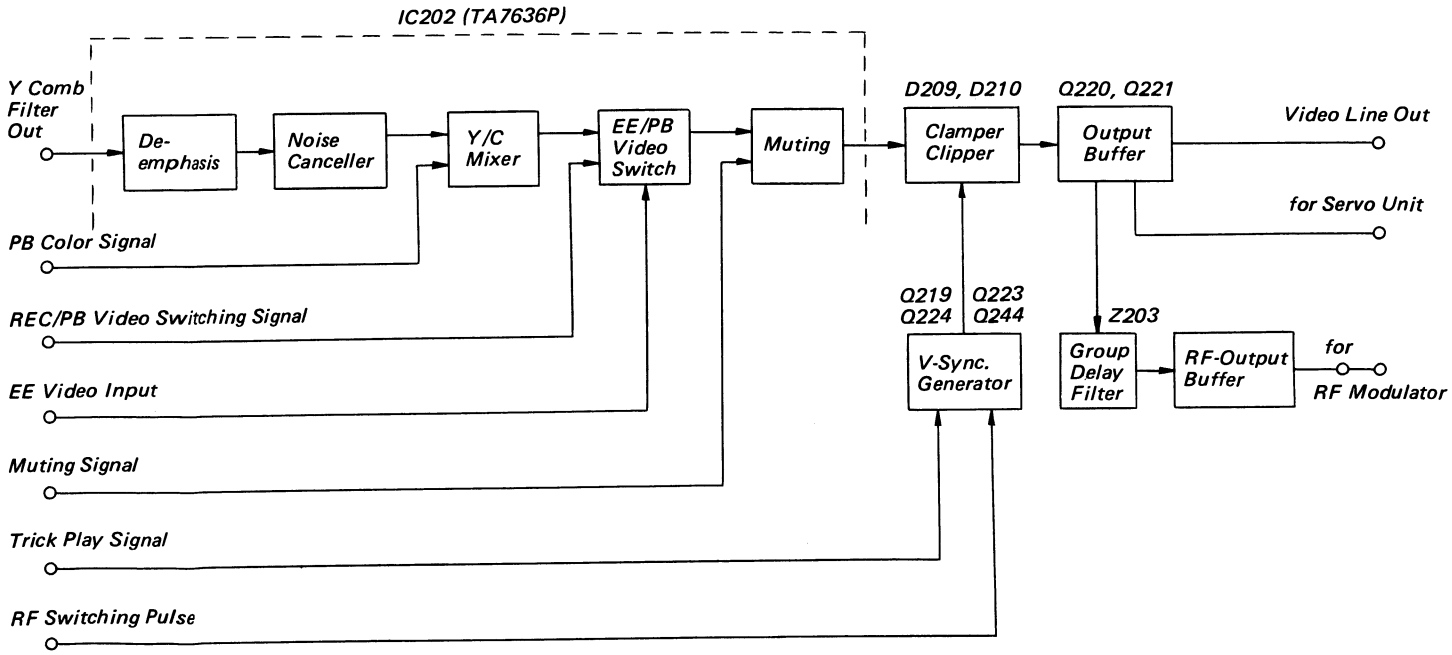



**Fig. 1-19 Luminance Signal Playback Circuit Block Diagram**

**(9) Vertical sync pulse inserting circuit**

The vertical sync pulse of the playback video signal exists about 7 H behind the head switching pulse as placed so in recording. If in still playback, a band of noises comes into the vertical sync period or if the band itself is detected as the vertical sync pulse by the TV set, it could cause the picture on the TV screen to fluctuate up and down. To dissolve such a problem, a dummy vertical sync period or if the band itself is detected as the vertical sync pulse by the TV set, it could cause the picture on the TV screen to fluctuate up and down. To dissolve such a problem, a dummy vertical sync pulse is forcibly buried into the vertical sync period. The burying position is not 7 H behind the head switching pulse, but about 4 H. The reason is that the dummy vertical sync pulse of 7 H behind is almost always at the same position as the actual vertical sync pulse. The TV set cannot identify which pulse is to be used for vertical synchronization, resulting in vertical picture fluctuation. To securely synchronize the TV picture only by the dummy vertical sync pulse, this is positioned in advance of the actual one.

In a special playback mode of operation, including the cue, review, or still, the special playback signal turns Q244 on, which in turn, allows the astable multivibrator, consisting of Q223 and Q224, to function. The astable multivibrator is triggered by the pulse formed in the way that the head switching pulse was differentiated by the circuit, consisting of C282 and R327. The astable multivibrator, then, produces a pulse of approximately 4 H wide at the cathode of D211. The pulse is passed through the differentiating network, consisting of C279, R313, and R314. The differentiated pulse keeps Q219 turned on for approximately 250 μsec every vertical sync interval to produce the dummy vertical sync pulse, which is buried into the video signal. A timing chart for the above operation is shown in Fig. 1-20.

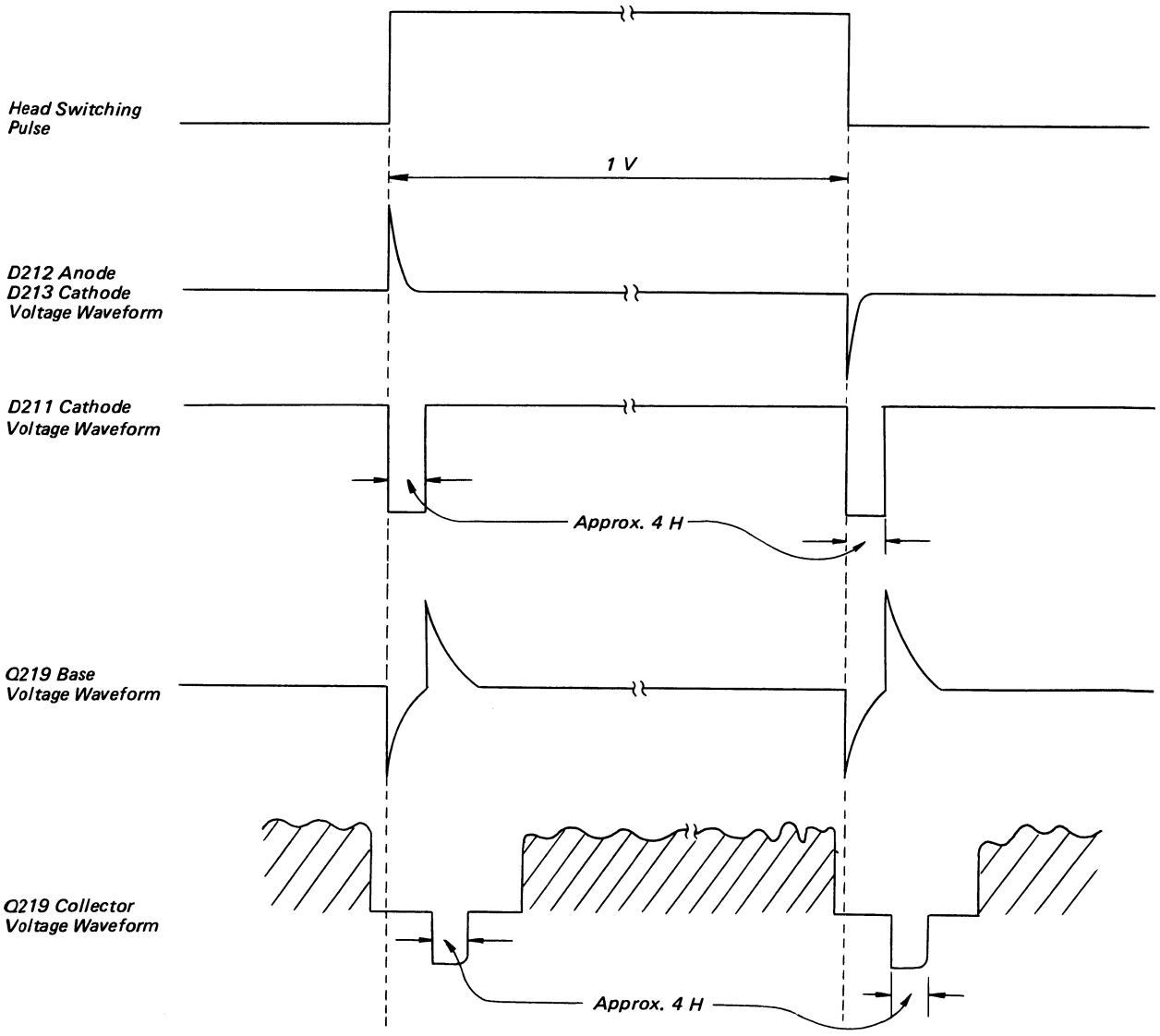



**Fig. 1-20 Vertical Sync Pulse Insertion Timing Chart**

**(10) Video signal output circuit**

After passing the clamping and clipping circuit and vertical sync pulse inseting circuit described previously, the video signal output of pin-3 on IC202 (TA7636P) enters the Darlington emitter follower, consisting of Q220 and Q221. It, then, is led to the VIDEO OUT pin jack P208 the impedance of which is made at 75 Ω by R315.

Also, the video signal output of the above-mentioned emitter follower serves for the RF modulator. It passes the group delay filter Z203 and then enters the other emitter follower Q222, which converts it a low impedance. The low-impedance video signal is fed out from pin-4 on P204 to the RF modulator. At the same time, the video signal of low impedance is fed from pin-1 on P216 to the Servo Control Circuit board PW2233 to obtain a servo control vertical sync pulse in recording.

### 1-1-4. Chroma Signal Processing Circuits

The chroma signal processing circuits use two ICs: CX188 and CX196. CX188 contains a record/playback switching circuit, an ACC (automatic chroma control), an ACK (automatic color killer), frequency converters, a chroma APC circuit, a 3.58 MHz crystal-controlled oscillator, and a burst gate circuit. CX196 contains a horizontal sync separator, an AFC, a 175 fH VCO, an $I^2L$ digital counter, a mislock detector, a frequency converter, and a carrier phase inverting switcher.

#### 1-1-4-1. Chroma signal function circuits

This section deals with the function circuits contained in and associated with IC245 (CX188) and IC246 (CX196). The C signal recording and playback processes will be described in Sections 1-1-4-2 and 1-1-4-3.

**(1) ACC, IC245**

The ACC circuit consists of ACC amplifier the gain of which is controlled by the input DC voltage, a burst gate circuit, a crystal-controlled oscillator, and an ACC detector. In recording the C signal applied to pin-6 on IC245 is amplified through the ACC amplifier, the output of which is fed to the ACC detector. The ACC detector, then, sync detects the C signal with the signal output of the 3.58 MHz crystal-controlled oscillator in the period of the burst gate pulse. The output of the ACC detector is a DC boltage in proportion to the burst level of the C signal. The output DC voltage is applied as the control signal to the ACC amplifier. As the ACC amplifier and ACC detector comprises a control loop, this makes constant the C signal level at the output of the ACC amplifier.

**(2) ACK, IC245**

This circuit detects the presence of the C signal by the DC level of the ACC detector circuit to output a color killer signal. The color killer signal switches the buffer so that in the color mode, the C signal from pin-11 on IC245 is added with 7.5 V DC and can be output and in the monochrome mode, no C signal with 0 V DC can be output.

**(3) Frequency converter I, IC245**

The C signal of 3.58 MHz which has been stabilized in the recording ACC circuit is balance-modulated to 688 kHz with the 4.27 MHz signal, which will be described later. The modulated signal is output from pin-24 on IC245 and in recording, is passed through the low-pass filter, consisting of C362, L226, and C363 to take out the 688 kHz C signal. The 688 kHz C signal is superimposed on the FM Y signal. In playback, it is converted to 3.58 MHz through the 3.58 MHz bandpass filter Z208. Note that when in recording, the ACK (automatic color killer) is in operation, the output at pin-24 on IC245 is DC voltage only.

**(4) 3.58 MHz crystal-controlled oscillator, IC245**

In recording, this oscillator is injection-locked by input of the burst and in playback, oscillates as the reference. In recording, a part of the output signal is fed to the above-mentioned ACC circuit and the remaining to IC246 to produce 4.27 MHz carrier. In playback, it is passed through the 90 degree phase shifter, comprised of L229 and C372, to the APC detector. Note that the output of the APC detector is not used in recording.

**(5) Record-playback switching circuit, IC245**

The playback +12 V voltage input to pin-7 prompts the switching circuit to switch over the C signal so that in recording, the C signal at pin-6 on IC245 feeds to the ACC amplifier or in playback, the C signal at pin-5 feeds to the ACC amplifier. Also, the playback +12 V voltage controls the switching circuit so that in recording, the ACC output signal from pin-12 can be taken out as the C signal at pin-11 or in playback, the C signal passed pin-13 and through the comb filter can be fed out from pin-11.

Further, the playback +12 V voltage turns the switching circuit in the IC "On" in recording or "Off" in playback to switch the 3.58 MHz crystal-controlled oscillator to be injection-locked or free oscillation, accordingly. It should be noted that with use of the switching circuit, only a single crystal can serve for C signal processing both in the recording and playback circuits.

The voltage detected in the ACC circuit is switched to store in C337 at pin-9 or C338 at pin-10 by the playback +12 V voltage and head switching pulse. In recording, the voltage is connected to pin-9 only and in playback, it is connected to pin-9 or 10 alternately at intervals of field by the playback +12 V voltage. In playback, that is, switching is done among the integrating capacitors for the ACC detector every head switching, thereby providing the function equal to that of two ACC circuits. This is required to prevent such a phenomenon that if there is an output level difference between the heads in playback, a signal of ACC output is involved in undesired transient due to switching the heads, resulting in color uneveness on the upper part of the playback picture.

**(6) Horizontal sync separator with equalizing pulse elimination, Q246**

The record/playback video signal is fed from pin-7 on IC202 through the low-pass filter, consisting of R419, R420, C348, and C347, to pin-17 on Q246. The horizontal sync separator in Q246, then, separates the horizontal sync pulse from the video signal and eliminates the equalizing pulse.

**(7) 175 fH VCO, IC246**

This Schmitt-type RC VCO is adjusted in the oscillation frequency with change of the time constant of R416 and C380 of charging or discharging by R353. The VCO is to be set to oscillate at 175 fH where the action points for the AFC and APC circuits are at the center when the DC voltage at pin-11 or 12 on IC246 is at the medium of the variable range.

**(8) 1/4 counter and frequency converter II, IC246**

The 175 fH signal of the VCO is 1/4 counted down to 688 kHz, which is mixed through the frequency converter II with the 3.58 MHz signal fed from IC245 (CX188) to produce a 4.27 MHz carrier.

**(9) 1/35 counter and AFC detector, IC246**

The 175 fH signal output of the 175 fH VCO is 1/35 counted down to 5 fH, which is transformed to trapezoidal wave through C344 and R425. The trapezoidal wave is sampled by the sync pulse having the equalizing pulse eliminated. The resulting error signal is passed through the AFC filter, consisting of C381, R415, C382, C383, and R414 to control the VCO.

**(10) Carrier phase inverting switcher, IC246**

This circuit phase-inverts the carrier frequency-converted to 4.27 MHz by the head switching pulse and fH/2, 50% duty signal every horizontal sync interval, and stops the phase inversion every vertical sync interval. The phase-inverted 4.27 MHz carrier is taken out from pin-2 on T203 and is applied to pin-1 on IC245 (CX188).

**(11) Mislock detector, IC246**

The mislock detector, consisting of a digital circuit, needing not usual burst ID circuit. In the $\beta$ Format system, it may sometimes happen that the 4.27 MHz carrier fails in the H interval phase inversion, resulting in considerable deviation of the VCO output frequency. This causes a sidelock phenomenon or too late APC recovering. The picture, then, is deteriorated uneven. To prevent this, the mislock detector having a counter and gate in combination feeds the signal of the APC circuit back to its input when the VCO output signal frequency and playback horizontal sync pulse frequency exceed the pre-determined range so that these may be quickly recovered to the correct frequencies.

**(12) HD pulse shaper, Q235**

The HD pulse shaper obtains a HD pulse without equalizing pulse of 5 $\mu$sec wide, approximately. It operates in the manner that the pulse appearing at pin-21 of the external time constant connection for the equalizing pulse eliminating circuit in IC246 (CX196) is differentiated at the trailing through C343 and R426 and is applied to the base of Q235, the collector of which feeds out the HD pulse. The HD pulse is fed to the Logic Circuit board PW2233 as well as the DC compensator in IC204 (TA7637P).

**(13) Burst expander, Q241, Q213**

In recording, the burst expander extends the burst alone of the C signal in the recording circuit to improve the signal-to-noise ratio of the C signal. Expanding the burst increases the signal-to-noise ratio of the APC loop in the playback circuit. The amount of burst expansion is 2 dB in the $\beta$II format or 6 dB in the $\beta$III format. In the $\beta$II format, Q241 is turned on only, where Q206 has R217 and R218 in series with and R203 in parallel with the emitter. In the $\beta$III format Q213 is turned on, where Q206 has R203 and R217 connected in parallel the emitter.

**(14) Burst compressor, Q234**

In playback, the burst compressor circuit compresses the burst that has been extended by the burst expander circuit in recording. The burst, however, tends to be made too low in the average as the chroma signal in the VCR is passed through a narrow band filter. The picture played back of such a playback signal through the TV set is rather thick in the saturation by the ACC. The color quality on screen the TV is decreased as viewed. To prevent this the burst in playback is held to be raised up 2 dB. In the $\beta$II format playback, that is, no burst compression is provided and in the $\beta$III format one, the burst is compressed -4 dB. In the $\beta$III format, the burst level is as high as 4 dB right after having passed the comb filter, as shown in Fig. 1-21 below. The burst level, therefore, is decreased -4 dB in the way that Q234 is turned on by the burst gate pulse. C278 compensates the burst for the phase in the $\beta$III format.

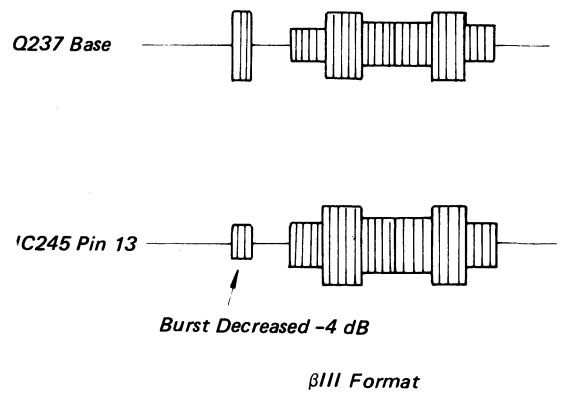



**Fig. 1-21 Playback C Signal**

### 1-1-4-2. Chroma Signal Recording Process

The C signal fed to pin-6 on IC245 (CX188) passes the ACC circuit, is frequency-converted with the 4.27 MHz carrier from pin-1, and passes the low-pass filter to take out the recording 688 kHz C signal. From pin-11, in addition, the C signal containing the color killer signal is fed out. The color killer signal, also, is fed to the luminance-chroma mixer in IC202 (TA7636P). Note that in recording, the luminance-chroma mixed signal is not used.

The signal output of the crystal-controlled oscillator is connected to pin-6 on IC246 (CX196) to frequency-convert to 4.27 MHz with a quarter (688 kHz) of the oscillation frequency of the 175 fH VCO that is AFC-controlled by the horizontal sync pulse. The frequency-converted 4.27 MHz signal passes the phase inverter to the frequency converter I. After this, the signal is processed as described previously. In the ACC circuit, the C signal and the signal of the crystal-controlled oscillator are used for synchronous detection. The horizontal sync pulse from pin-20 on IC246 is delayed through C339, L225, and C340. During the burst gate period the ACC action makes the ACC output level constant. The C signal recording process is illustrated in Fig. 1-22.

### 1-1-4-3. Chroma Signal Playback Process

The 688 kHz C signal fed to pin-5 on IC302 (CX188) passes the ACC circuit. The signal output of the ACC circuit is frequency-converted with the 4.27 MHz carrier fed from pin-1 to 3.58 MHz. The 3.58 MHz is fed out from pin-24 through the 3.58 MHz bandpass filter to the comb filter. In playback, the C signal that was phase-inverted in recording is recovered to continuous signal. After passing the comb filter, the crosstalk component of the chroma signal is eliminated. This process was described in detail in Section 1-1-3 the "Luminance Signal Processing Circuit".

The signal which passed through the comb filter passes the burst compressor in the βIII format and then returns to pin-13 on IC245 and is fed to the ACC detector, color killer, and APC detector. The APC detector has two input signal of which phase is shifted 90 degrees as it is locked. For the reasons, the signal output of the crystal-controlled oscillator is passed through L229 and C372 to shift 90 degrees and then is connected to the APC detector. This makes the C signal coincide in phase with the signal of crystal-controlled oscillator and allows ACC synchronous detection together.

The APC detected voltage passes the APC filter, consisting of C331. C330, R428, R429, and C326, to pin-11 on IC246 (CX196) to control the 175 fH VCO for compensating the C signal for possible phase deviation. In event of too much phase deviation or side-lock, the mislock detector functions so that the error voltage may be charged into C388. This returns the APC to the normal operating point quickly.

With respect to the ACC output signal, this is processed as in recording. The C signal containing the color killer signal fed from pin-11 on IC245 is fed to the Y-C mixer at pin-10 on IC202 (TA7636P). The color killer makes low the level at pin-11 on IC245. This turns Q247 on, which disconnect the C signal. The C signal playback process is shown in Fig. 1-23.

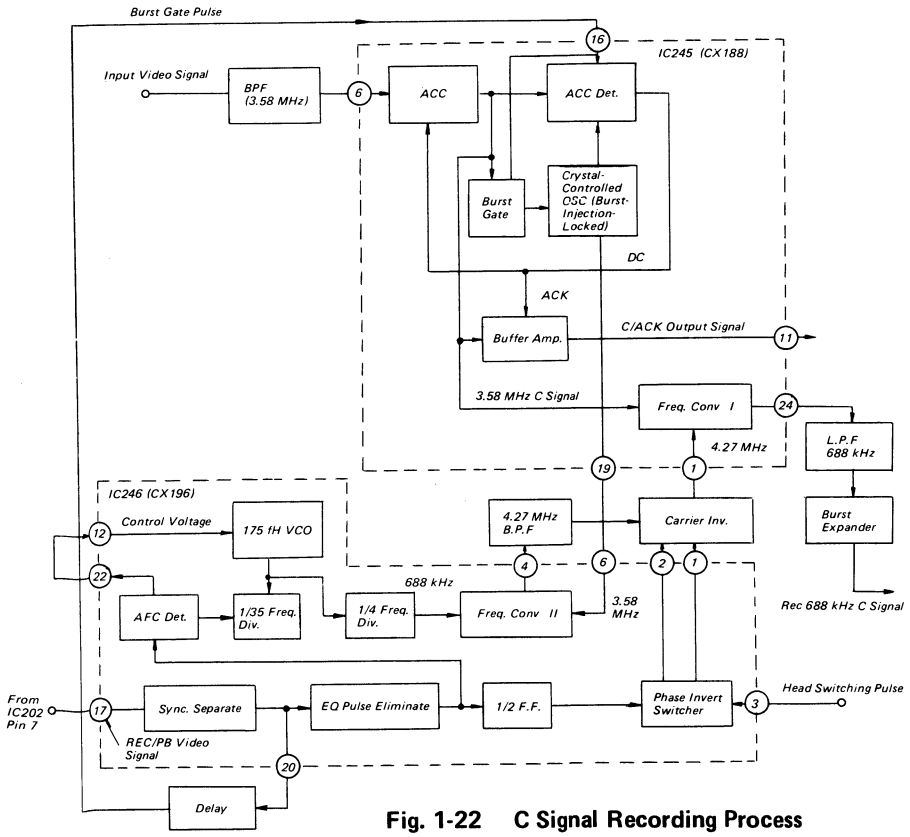



**Fig. 1-22 C Signal Recording Process**

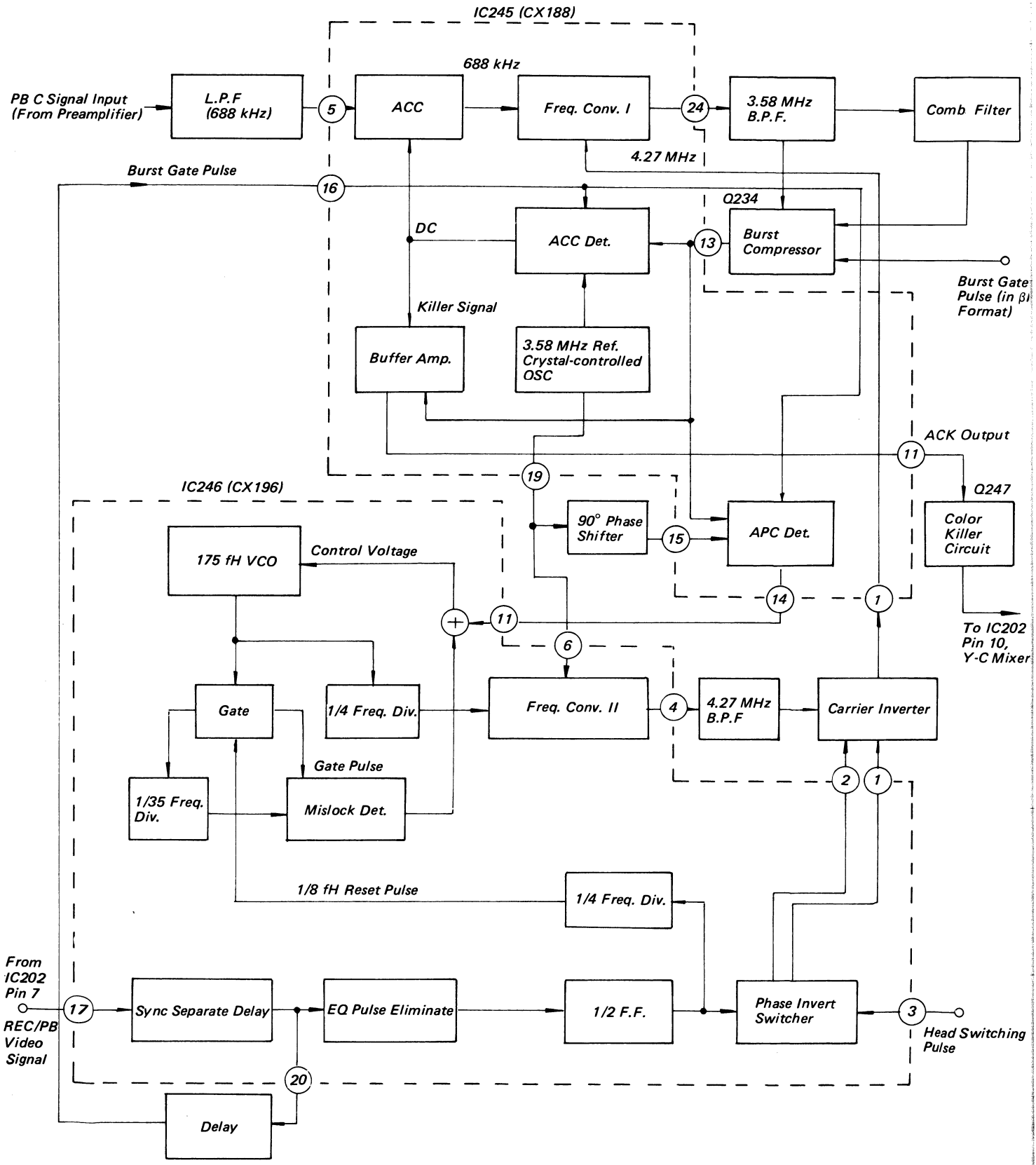



**Fig. 1-23 C Signal Playback Process**

## 2-1 SERVO SYSTEM

### 2-1-1 General

This Servo Control Circuit, consisting chiefly of an N NOS IC (TM4217P), is contained in a half part of the board PW2233. It includes the following circuits.

A head servo circuit that governs the phases of the video heads and controls the head motor driving the reel tables, and a head motor drive circuit.

A capstan servo circuit that keeps the tape at a specified speed and controls tracing of the video heads in a correct phase relationship on the tape pattern in the playback mode of operation, and a capstan motor drive circuit.

A super scanning circuit that controls the relative speed of the tape to the video heads to provide a capability of picture search at either of two speeds as high as approximately ten times (normal search speed) the regular playback speed and approximately thirty times (high search speed).

A double-speed circuit that allows playback at a speed as high as two times the regular playback speed with the capstan servo circuit locked.

A vertical sync separator circuit, muting signal generator circuits, and others.

The LSI (TM4217P) used in the Servo Control Circuit provides the following features as compared with previous LSI (TM4216P).

The reference clock is taken from the 3.58 MHz crystal-controlled color oscillator in the Video Circuit, while it was produced by the specifically-designed 7.19 MHz crystal-controlled oscillator in the previous LSI.

The capstan PG frequency divisions are 1/2 and 1/3 in connection with the use of the new βIII Format, while they were 1/2 and 1/1 in the previous LSI. The former results in the removal of the external frequency divider circuit.

A new built-in switching circuit is used to switch the PG and control pulse frequency division from 1/1 to 1/2 at the same time, allowing the above-mentioned double-speed playback.

As pointed out above, the new servo LSI improves the servo control capabilities without expanding the external circuits.

Inside the servo LSI, all the signal processes and generations are carried out in the digital fashion. The head motor used, which is a brushless direct-drive motor, revolves the heads and drives the reels. The capstan motor used is a DC motor having a set of brushes. The functional circuits of the Servo Circuit are described in some detail in the following sections.

### 2-1-2 Video Disk Servo Circuit

Fig. 2-25 shows the phase relationship between, on the time chart of, the pair of video heads and 30PG coil. For the block diagram, see Fig. 2-24. The operation of the video head servo circuit is as follows.

The pair of the video heads are controlled in a fixed-phase servo control manner. That is, the DC, 3-phase, 8-pole Hall motor directly drives the video head assembly. Revolution of the video head assembly induces a pair of PG pulses that respond exactly to the movements of the video heads. In the recording mode of operation, the PG pulses are detected and compared in the phases with the vertical sync pulse separated from the recording video signal to keep the video heads at a constant speed, while in the playback mode of operation, the PG pulses are detected and compared with the reference trapezoidal wave composed of the clock pulse produced in IC501 to maintain the video head rpm at the constant speed.

The cylinder assembly consists of a fixed upper cylinder, a rotary video head assembly, a fixed lower cylinder. The rotary video head assembly has the pair of video heads A and B and a couple of magnets placed on the video head disk, the pair and couple each being 180 degrees apart the other. The lower cylinder has the PG coil placed. The PG coil develops a couple of PG pulses whenever the couple of magnets passes over the PG coil. The developed PG pulses are used as the tack pulses for the video head servo control. The PG pulses, also, are used to produce RF switching pulses for use of alternately switching over the video heads and for other purposes. Details of the video head servo circuit will be described in the following sections.

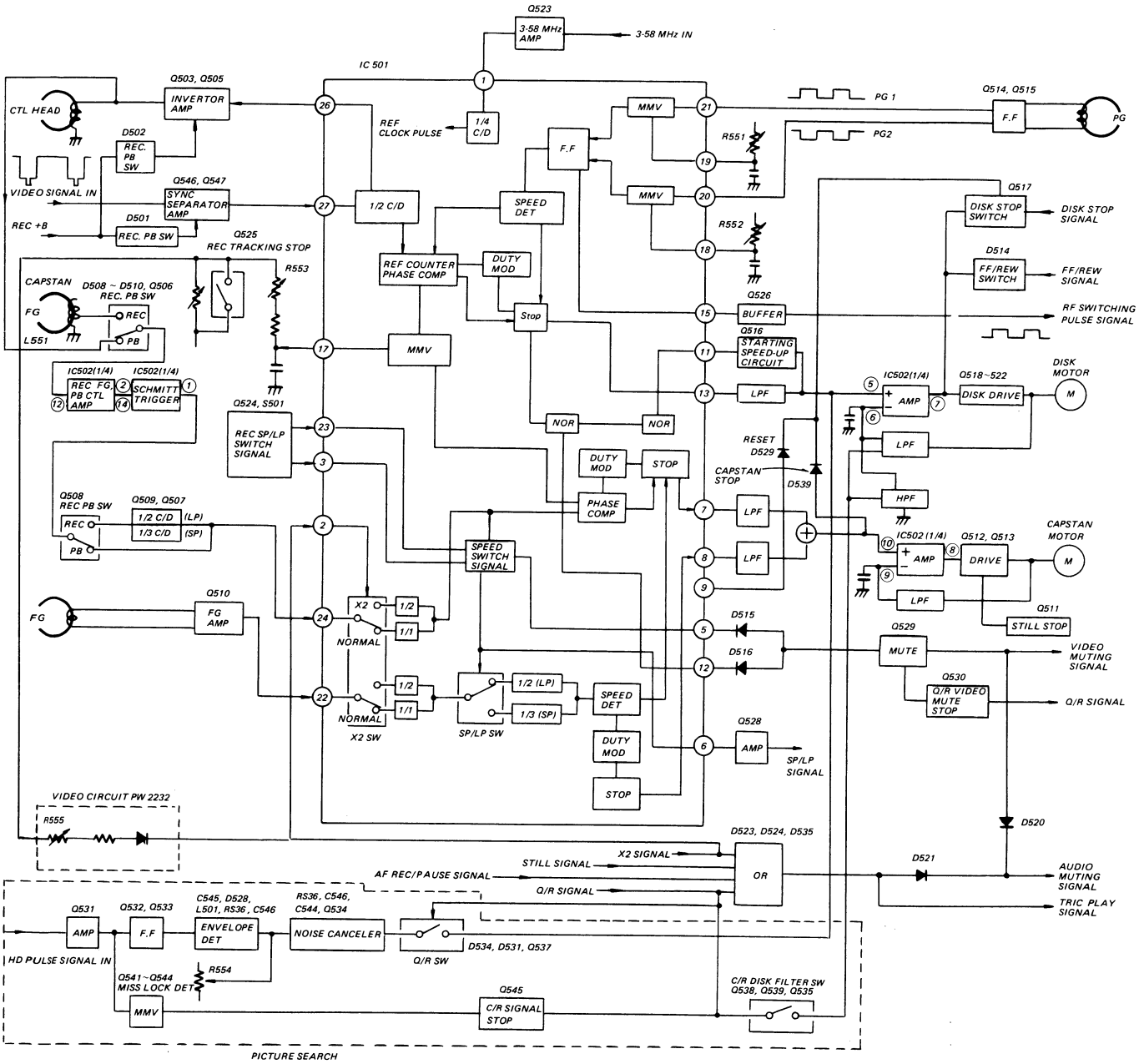



**Fig. 2-24 Servo Circuit Block Diagram**

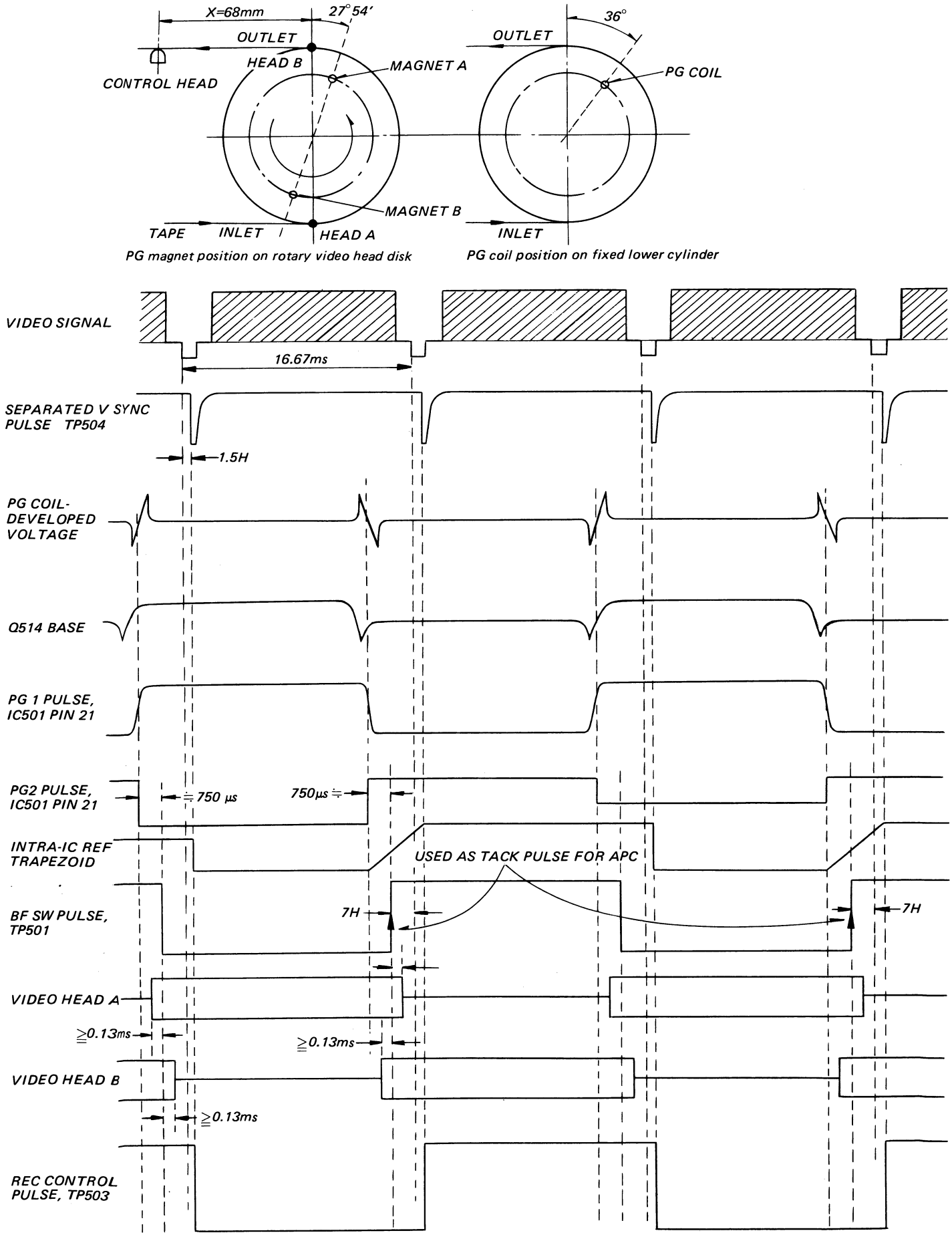
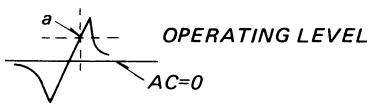



**Fig. 2-25 Time Chart Illustrating Phase Relationships Between Video Heads and PG Magnets in Recording Mode of Operation**

**(1) PG Pulse Circuit**

The couple of PG magnets and coil, which are positioned as illustrated in Fig. 2-25, develop PG pulses that exactly respond to the video head movement. The two PG magnets on the video head disk are different in the polarity. The voltage developed in the PG coil, by one PG magnet is opposite to the voltage by the other when the respective PG magnets come near and go away the PG coil. The PG pulse by one PG magnet is shown in Fig. 2-25 as observed across the PG coil on an oscilloscope. The actual PG pulse waveform has the upper part suppressed as one end of the PG coil is connected to the base of Q514. Fig. 2-26 is a PG pulse amplifier circuit.

When a voltage is applied to the disk motor. This starts the video head disk, which makes the PG coil develop the PG pulse. The PG pulse enters the PG pulse amplifier circuit successively. The connection of the R571 and R572 is present at around 0.4 V. If the first PG pulse having a waveform as

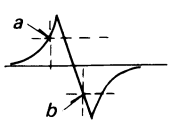



comes in, the descending edge of Q514 does not turn on Q514. When the base voltage of Q514 exceeds the operating level around point *a* of the ascending edge, Q514 is turned on. This, then, drops the base voltage of Q515 down to 0 V, the collector voltage rising up. The result is that the connection voltage of R571 and R572 becomes the value to which the line voltage is divided by a parallel of R571 and R575 plus R573 and R572. The resistor values are selected so that the connection voltage may be approximately 1.4 V, which keeps Q514 turned on.

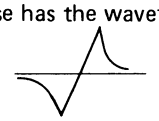
In turn, when the second PG pulse of opposite polarity having such a waveform as


comes in, the ascending edge does not change the state of Q514 which has been on. The descending edge drops the base voltage, or the above-mentioned 1.4 V voltage, of Q514 down to, the OFF level. This turns Q514 off, which allows current to flow through R574 and D536 into the base of Q515 to turn on. The connection voltage of R571 and R572 becomes the value to which the line voltage is divided by R571 and a parallel of R572 and R573. The resistor values are selected so that the connection voltage may be at the OFF level for the base of Q514. Thus, Q514 keeps turned off. The PG pulse amplifier repeats the on-off operation afterward; that is, it operates as the so-called Schmitt trigger.

If the first PG pulse having the waveform as comes in,

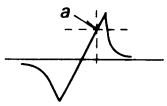



the ascending edge turns Q514 on at point *a*. The connection voltage of R571 and R572 becomes a value to which the line voltage is divided by a parallel of R571 and R573 plus R575 and R572. The subsequent descending edge drops at point *b* the base voltage of Q514 down to the OFF level for the base of Q514, which is turned off. This turns Q515 on and this keeps on until the succeeding PG pulse comes in. As the succeeding PG pulse has the waveform as

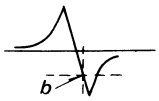


the ascending edge turns Q514 on, which turns Q515 off. These states are kept until the succeeding pulse comes in.

In short, Q514 is turned on by one PG pulse waveform as




at point *a* and it turns Q515 off irrrespective the polarity of the first PG pulse; and, Q514 is turned off by another PG pulse waveform as




At point *b* and it turns Q515 on.

The high collector levels of Q514 and Q515 determine the tracing periods of the heads A and B, respectively. The zener voltage of D536 deviates the Q515 off- and on-instants in reference to the Q514 on- and off-instants to make the Q514 and Q515 connector crosspoint voltage for the PG 1 and PG 2 pulses input to IC501 higher than the threshold level of the IC, as shown in Fig. 2-27. If the crosspoint voltage is too low, this adversely affects the logic operation of the IC. The capacitor C555 bypasses possible radio-frequency noises induced in the PG coil by the magnetic flux of the video heads and the like. One of the two PG pulses is used as the detection pulse for a splicing recording.

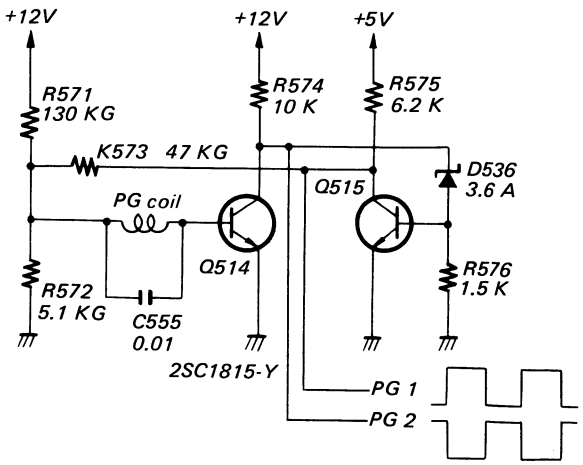



**Fig. 2-26 PG pulse Amplifier Circuit**

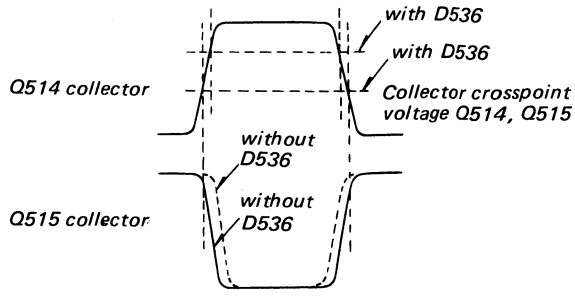



**Fig. 2-27 Effect of D536**

**(2) PG Pulse Delay, Phase Detector, and RF Switching Pulse Generator Circuits**

These circuits are contained in IC501 (TM4217P). The PG 1 and PG 2 pulses input to pins 20 and 21 on IC501 are delayed approximately 750 μsec at their respective trailing edges through the internal monostable multi-vibrators and time constant circuitries of R551 and C531 and R552 and C532. Note that the delay time is to be adjusted in playback with use of a master tape so that the leading edge of the RF switching pulse may be 7 Hs behind the playback vertical sync pulse VD. With the delay of the PG pulses, a RF switching pulse is formed which rises up at the time of the delayed trailing edge of the PG 1 pulse at pin 21 and drops down at the time of the delayed trailing edge of the PG 2 pulse at pin 20. The leading edge of the RF switching pulse is used as the tack pulse for the video head APC action either in the recording or playback mode of operation. The leading and trailing edges, also, are used for switching the video heads A and B, for detecting the head revolution, and others. The RF switching pulse is fed from pin 15 on the IC through the buffer transistor Q526 to the respective circuits.

In the recording mode of operation, the phase comparator circuit compares the leading edge of the switching pulse with the phase of the vertical sync pulse separated from the recording video signal. In the playback mode of operation, it compares the leading edge with the phase of the reference trapezoidal wave formed of the reference clock delivered from the Video Circuit. The signal resulting from the phase comparison is processed in a digital fashion. The timing relationship on the slope of the trapezoidal wave is shown in Fig. 2-28.

There is in the IC an additional speed detector which detects the period of the switching pulse. The speed detector makes the phase comparator produce a low level output, a high level output, or a trapezoidal wave according as the switching pulse frequency is out of, within, or at 30 Hz ±1.7%. In the steady state, therefore, the leading edge of the switching pulse is always locked on the slope of the trapezoidal wave. The 1.7 kHz duty modulation output corresponding to the position on the slope is held until the leading edge of the next switching pulse comes in. In the duration, the output voltage is integrated and applied to the positive end of the operational amplifier in IC502. The negative end has the sum of the voltage divided by R583 and R584 and the voltage fed back from the disk motor. The integrated voltage at pin 13 balances at the phase locked on the trapezoidal wave at any time so as to be equal to the sum of the voltages.

Therefore, in the recording mode of operation, therefore, the phase of the switching pulse leading edge is determined in terms of the voltage at the negative and of the operational amplifier (IC502, pin 6) as referenced to the recording vertical sync pulse. This means only that the phases of the video head B and the vertical sync pulse are relatively determined.

But, the vertical sync pulse cannot be determined yet as to where it is recorded on the tape. As for the phase of the video head A which is not servo-controlled, also, it is still not specified. The switching pulse and the video heads A and B are adjusted is the phases by playing back the master tape on which the vertical sync pulse is recorded in the connect position. The switching pulse leading edge is locked at the same position on the slope of the trapezoidal wave formed in the same time relationship both in the recording and playback time in which the PG pulse is converted to the switching pulse is varied to adjust the phase of the playback vertical sync pulse of each video head A or B in reference to the switching pulse. This allows the vertical sync pulse to be also recorded at the same position as the master tape. The noise due to head switching in playback, also, can be hidden out of the effective picture area on the bottom of the screen.

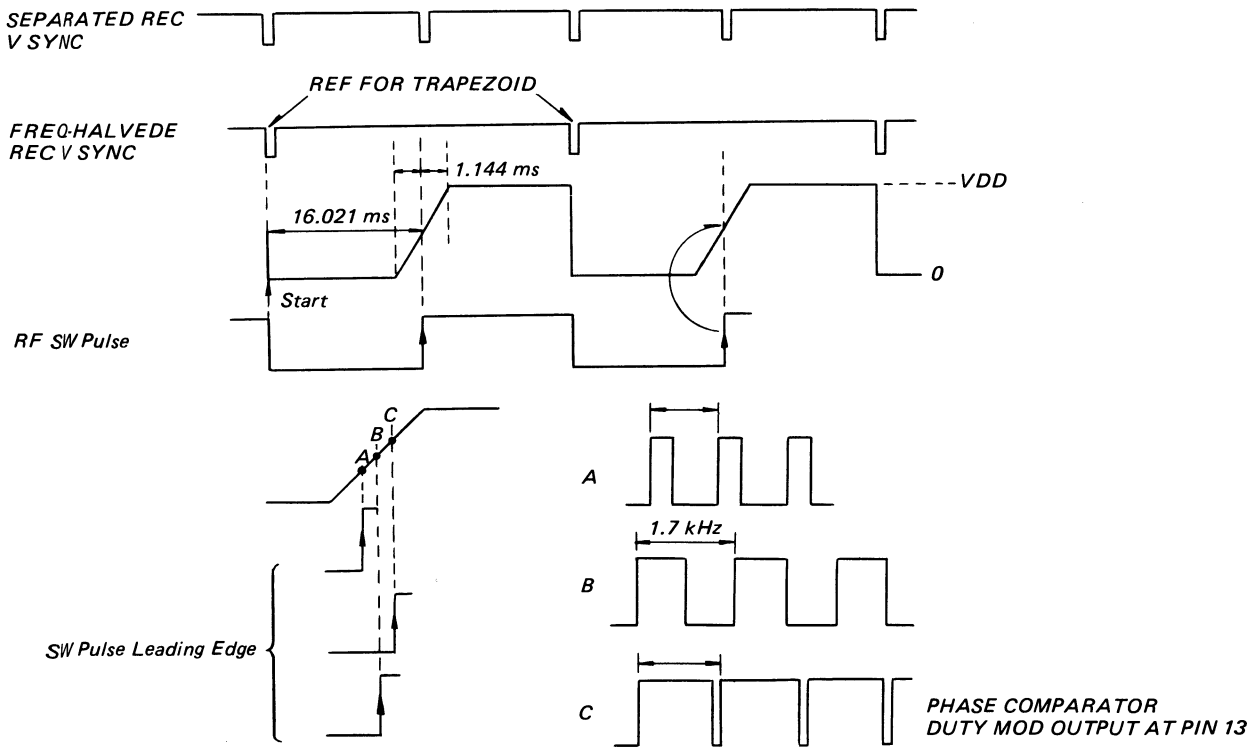



**Fig. 2-28 Phase Comparator Time Chart**

**(3) Disk Servo System Phase Compensation and Disk Motor Drive Circuits**

The disk servo system likely oscillates unless a phase comparison is provided since it has the phase detection loop only. It, also, needs to have a low-pass filter which smooths the detected output of the 1.7 kHz duty modulation to eliminate the carrier component.

The disk servo system is made stable by R580, C526, R587, and C527 and has R579, C525, and C528 to eliminate the carrier component. The detected voltage is smoothed and applied to pin 5 on IC502. The smoothed voltage is compared with the reference voltage is compared with the reference voltage at pin 6. The difference voltage is fed out of pin 7 to the negative feedback amplifier, consisting of Q518 through Q522, which magnifies it. The emitter voltage of Q520 controls the current flowing through the winding of the disk motor so that the revolutional phase of the pair of video heads assembled together with the disk motor should coincide with the reference phase.

The capacitor C526, which is connected to the +B line with the POWER switch turned on, is to have current charged quickly to raise the voltage at pin 5 on IC502, thereby facilitating the disk motor to revolve. The base of Q516, connected to pin 11 on IC501, is set to the low voltage when the switching pulse frequency is out of 30 Hz ±1.7%. It is set to the high voltage when the frequency is within the range. Such level changes adjust the current charged into and discharged from C526 which takes the longest time for charging and discharging. This is needed to shortens the starting and speed reducing times of the disk motor.

In any mode of operation except picture search, Q538 is open, D531 is reverse-viased, Q536 is on, and Q535 is on. In picture search, they are in the opposite states. Their functions will be described in the "High-Speed Picture Search Circuit" section.

The disk motor is stopped by Q517 in the way that the disk motor stop signal output of the Logic Circuit, when becoming high, turns Q517 on. In stopping, the voltage at pin 9 on IC501 is set to the low level. This makes high the capstan phase detection voltage at pin 7 on IC501, the capstan speed detection output at pin 8, and the disk motor phase detection output. These level changes charge their respective output capacitors. The charged capacitors assure that the motor control voltage can be securely applied to the disk motor to revolve when the disk motor stop signal becomes low. The diodes D529 and D542 are placed to disconnect pin 9 on IC501 from the disk motor operational amplifier output voltage while Q517 is off, or the disk motor is revolving.

Fast-forward (FF) or rewinding (REW) of the disk motor is set by D514 and R590. The connection of them is open either in the fast-forward or rewinding mode of operation only. It is at the low level in any other mode. The divided voltage at the connection of R590 and R588 is applied to the base of Q518, which saturates the output transistor Q519. The voltage level at one end of R588, or at pin 7 on IC502 is held low as the low level at pin 13 on IC501 is due to the disk motor revolutional frequency of approximately 4,000 rpm. The disk motor, then, revolves the reels at a high speed through the belt and planetary gears. One of the reels winds or rewinds the tape.

The disk motor may cause some wow and flutter every turn of revolution cannot be reduced by any circuit technique as only one phase comparison PG pulse can be detected during the turn of revolution. The wow and flutter may appear as jitter on the screen unless the HD pulse intervals either in the recording or playback mode of operation should be identical. For obtaining the identical HD pulse intervals, the disk motor used is designed so as to minimize the wow and flutter as well as its moment of inertia is made large.

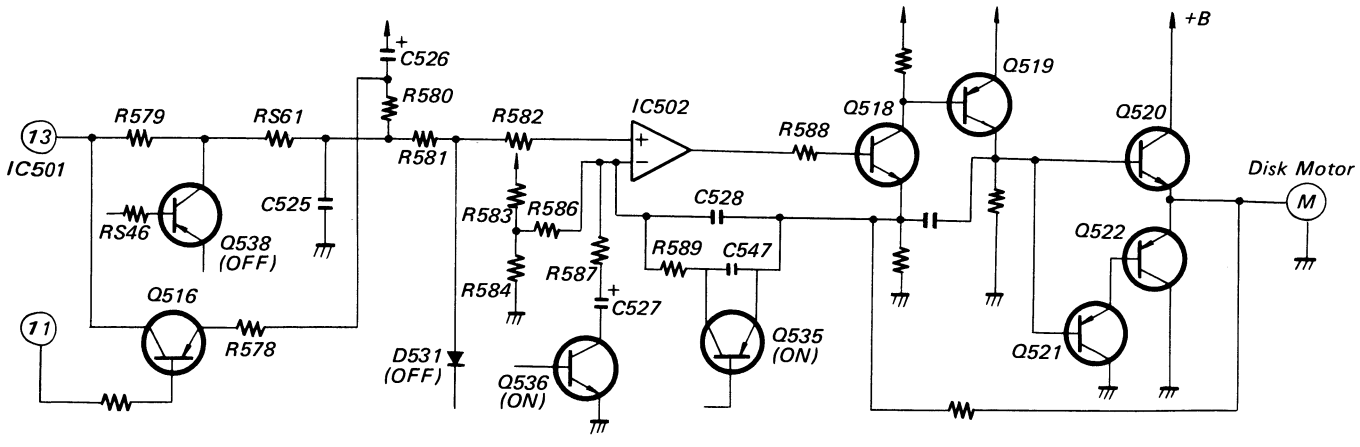



**Fig. 2-29 Disk Servo System Phase Compensation and Disk Motor Drive Circuits**

**(4) Recording Vertical Sync Separator and Internal Reference Signal Oscillator Circuits**

All the timing operations in the V-8000 are based on, or referrenced to, the output of the 3.58 MHz crystal-controlled oscillator located on the Video Circuit board. IC501 uses a 895 kHz clock which is derived from the 3.58 MHz reference signal (= 7.19 MHz ÷ 8 = 3.58 MHz ÷ 4). The IC counts the clocks to form the reference trapezoidal wave and other waves.

The 3.58 MHz signal, which has a 0.65 Vp-p sine wave, is input to the grounded-emitter amplifier Q523 to magnify. The transistor Q523 is needed to provide an amplitude of the signal enough to activate the succeeding frequency-divider stage as the present IC (TM4217P) has a waveforming shaping circuit only, while the previous IC (TM4216P) has a feedback crystal-controlled oscillator. The amplified signal is connected to pin 1 on IC501.

In the playback mode of operation, all the servo-operations are referenced to the clocks. In recording, an additional vertical sync pulse separated from the video signal is used. This was illustrated in the time chart in Fig. 2-25. The vertical sync pulse separator is provided specifically for the video head servo-operation to extract the vertical sync pulse only. The video signal is fed from the emitter of the final transistor stage in the Video Circuit, having an amplitude of 2 Vp-p as measured from its top. The first transistor stage Q546 in Fig. 2-30 extracts both horizontal and vertical sync pulses. The integrating network consisting of R504, C503, R505, and C504, further, extracts only the vertical sync pulse, which turns Q547 on. As the integrating network starts integration from the leading edge of the horizontal sync pulses, it takes approximately 1.5 H after the leading edge that the level at pin 27 on IC501 becomes low.

The series of D501 and R548 is placed to lock the level at pin 27 at the low level in the playback mode of operation. The capacitor C502 removes the impulse noise of the video signal. C505 is a speed-up capacitor. C506 prevents an integrated voltage noise due to turn-on of Q547 from entering pin 27.

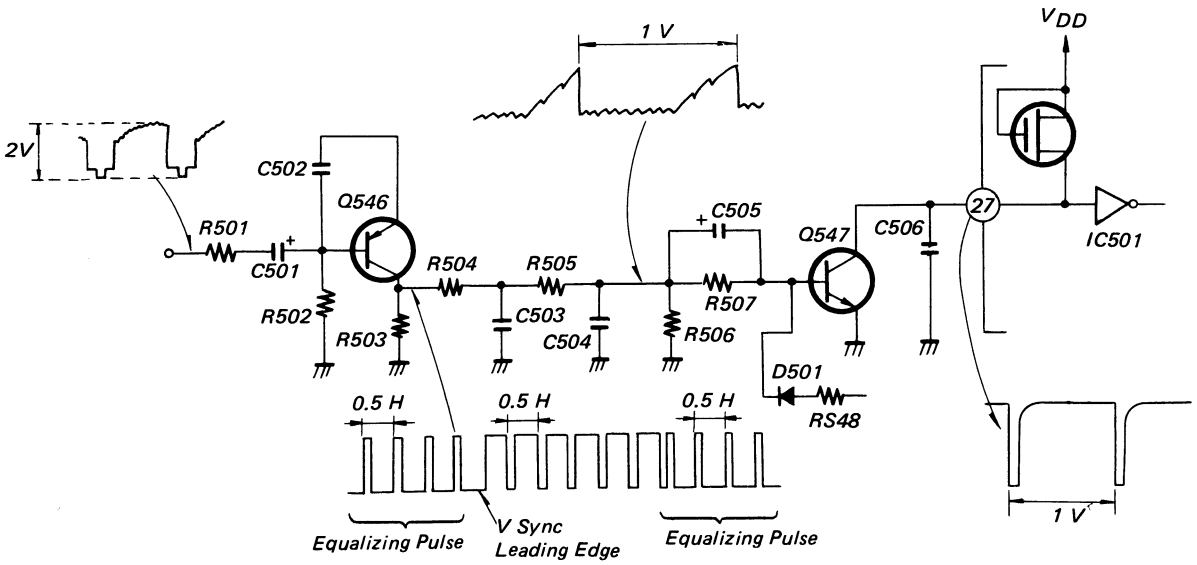



**Fig. 2-30 Vertical Sync Pulse Separator Circuit**

### 2-1-3 Capstan Servo Circuit

The capstan is driven by the capstan motor through the belt and pulley. In the recording mode of operation, the capstan servo circuit controls feeding the tape at a specified speed; in the playback mode of operation, it picks up the pulse put on the control track in recording to servo keeping the phase relationship between the video head revolution and the picked-up pulse as the tracking servo circuit. In the present capstan servo system, the capstan motor has a FG put on and also the capstan flywheel has another FG. The pulse developed from the flywheel is frequency-divided for use as the tack pulse for the APC in recording as the case with the control pulse in playback. Such a use of the FG pulses is advantageous in that in recording, the capstan needs not to precisely adjust the belt, pulley, and any other mechanical device, but the FG pulses are always at the frequencies determined in a digital way in IC501. The determined capstan motor FG pulse frequency is 12 pulses per revolution and the capstan flywheel FG pulse frequency is 42 pulses per revolution. The revolutional frequencies and frequency divisions of the capstan flywheel and capstan motor are shown in Fig. 2-31.

The capstan servo system makes use of a double control loop, consisting of an APC and AFC loops, as the capstan motor revolutional frequency is switched to change the tape speed and a rather higher system stability can be obtained. The sum of the two loop error voltages is used to drive the capstan motor. Details of the capstan servo circuit will be described in the following sections.

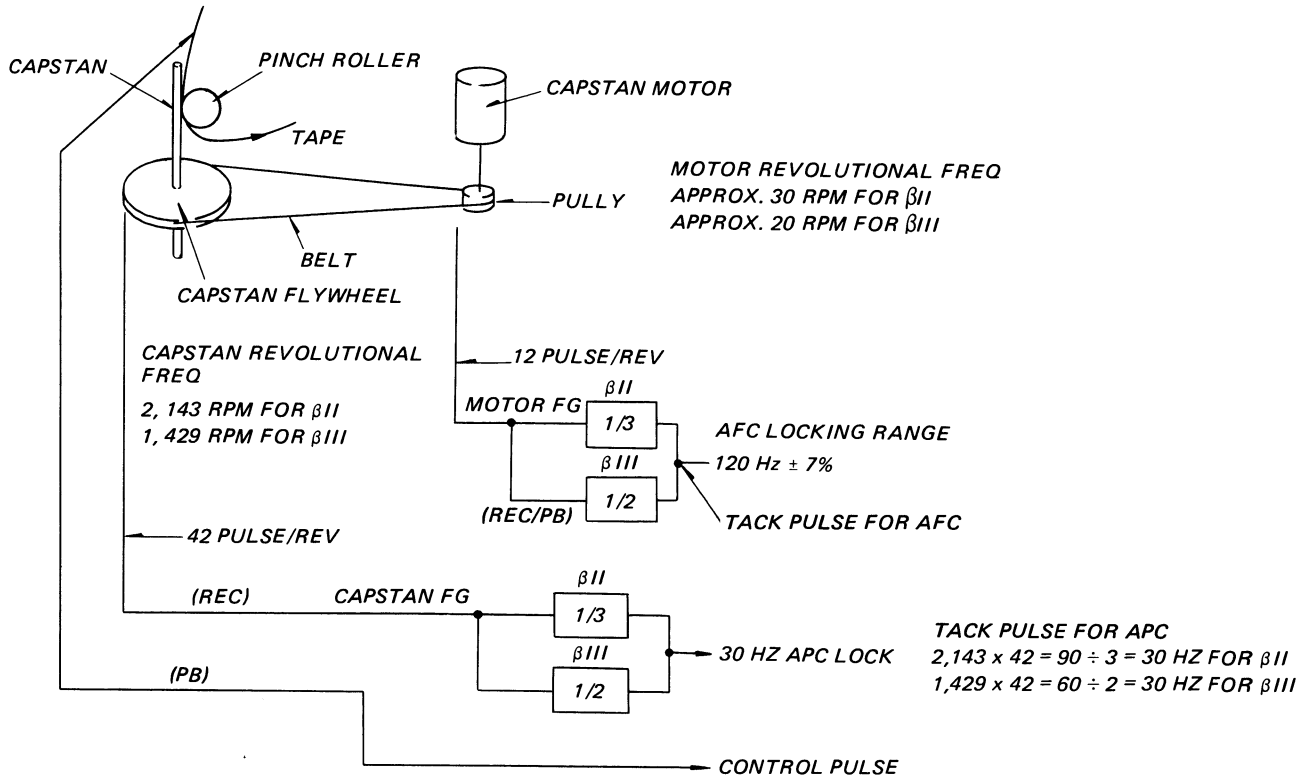
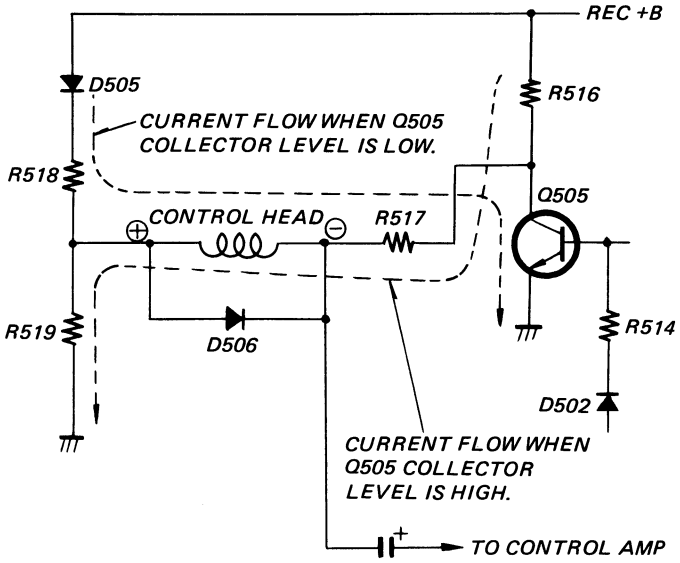



**Fig. 2-31 Capstan Motor Drive Circuit with Frequency Dividers**

**(1) Recording Control Pulse Processing and Capstan FG Signal Processing Circuits; Playback Control Pulse Amplifier and FG Signal Processing Circuits**

The tack pulse for the AFC, as described above, uses the FG signal developed by the capstan motor and the tack pulse for the APC is the capstan FG signal by the capstan flywheel in recording or the recorded control pulse in playback. These pulses are explained in details below.

In playback, the tape feed phase and the video head revolutional phase must be made to coincide; otherwise, normal picture cannot be reproduced. In recording, therefore, the current of square wave obtained by half-counting down the vertical sync pulse is made to flow into the control head to staturate. The direction of the square wave current is determined so that when played back, it can be positive at the beginning of tracing by the video head A and can be negative at the beginning of tracing by the video head B. The polarity of the switching pulse and the square wave at pin 26 on IC501 are determined in IC501. It must be inverted and amplified by Q503 and Q505 in accordance with the above-mentioned current direction rule for the control head. The voltage having such a polarity is applied to the control head to make current to flow in a DC fashion, by use of the circuit as in Fig. 2-33.




**(Control Current Recording Circuit)**

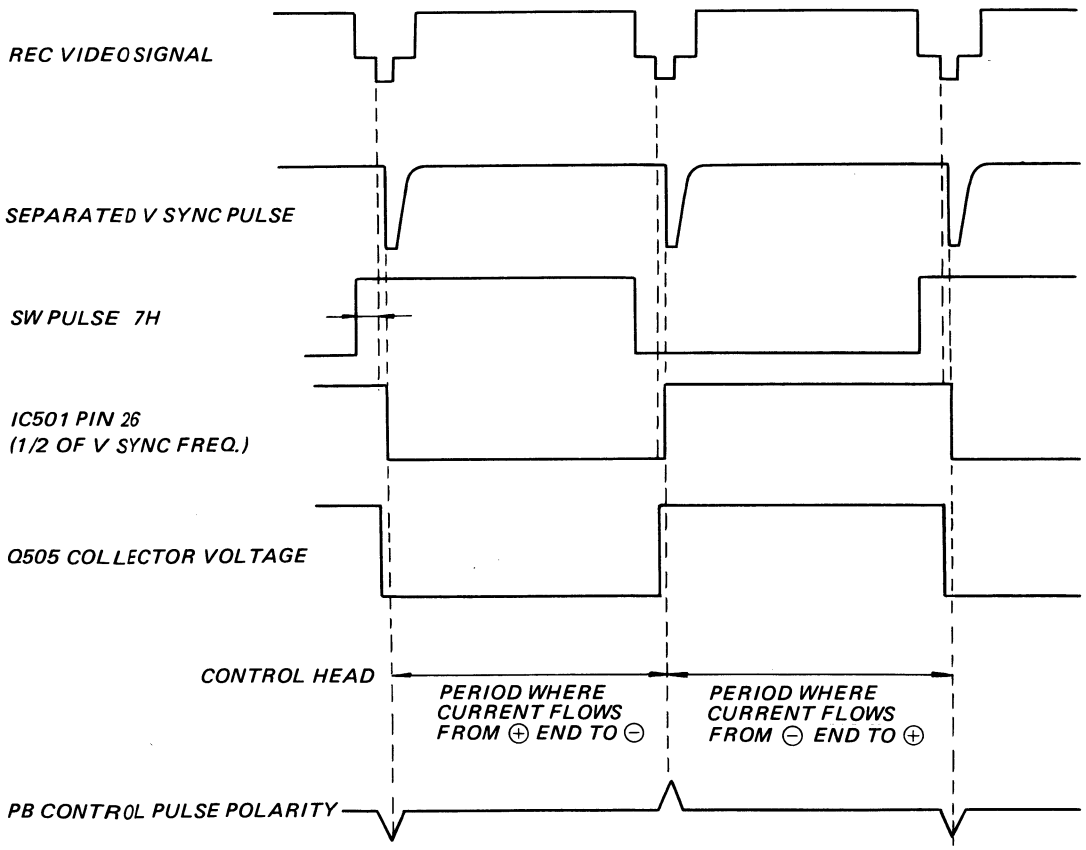



**Fig. 2-33 Phase Relationship Between Control Head Recording Current and Associated Signals and Control Current Recording Circuit**

As shown in the figure, the current flowing through the control head changes according to the level at the collector of Q505, high or low. The connection of R518 and R519 is present at approximately 5 V by selecting their values. At the time when the collector level of Q505 becomes high, the collector of Q505 has a voltage, approximately 10 V, to which the recording +B voltage is divided by R516, R517, the control head impedance, and R519. The current flowing through the control head from the ⊖ end to ⊕ is approximately 1 mA, which results from the fact that the potential difference between the collector voltage of Q505 and the connection voltage of R518 and R519 is divided by the sum of the control head impedance and R517. At the time when the collector level of Q505 becomes low, also, the control head has the same potential difference across this, resulting in current flow of approximately 1 mA from the ⊕ end to ⊖. The control head, then, is ssaturated and records the pulse on the tape.

When the current flow changes, this may cause an undesired transient voltage to be developed across the control head by its inductor. The diode D506 prevents the transient from affecting the other circuits. D505 prevents possible noise from the recording +B line from fluctuating the voltage at the ⊕ end of the control head. D502 and R514 do turn Q505 on completely in playback so that the voltage at the ⊖ end cannot fluctuate. Note that D506 does not allow a forward current to flow. The reason is that the voltage which is the product of the head current by the head impedance is not high enough to allow D506 to conduct the forward current.

In turn, the following describes the capstan FG signal processing circuit and playback control pulse amplifier circuit. As described previously, the capstan FG signal obtained from the capstan flywheel is recording is used in a similar way to that of the control pulse in playback. Therefore, a circuit is required which switches the input depending on the operation mode, recording or playback, amplifies and shapes it to square wave so as to enable the input circuit at pin 24 on IC501 to operate. The circuit for such operations is shown in Fig. 2-34.

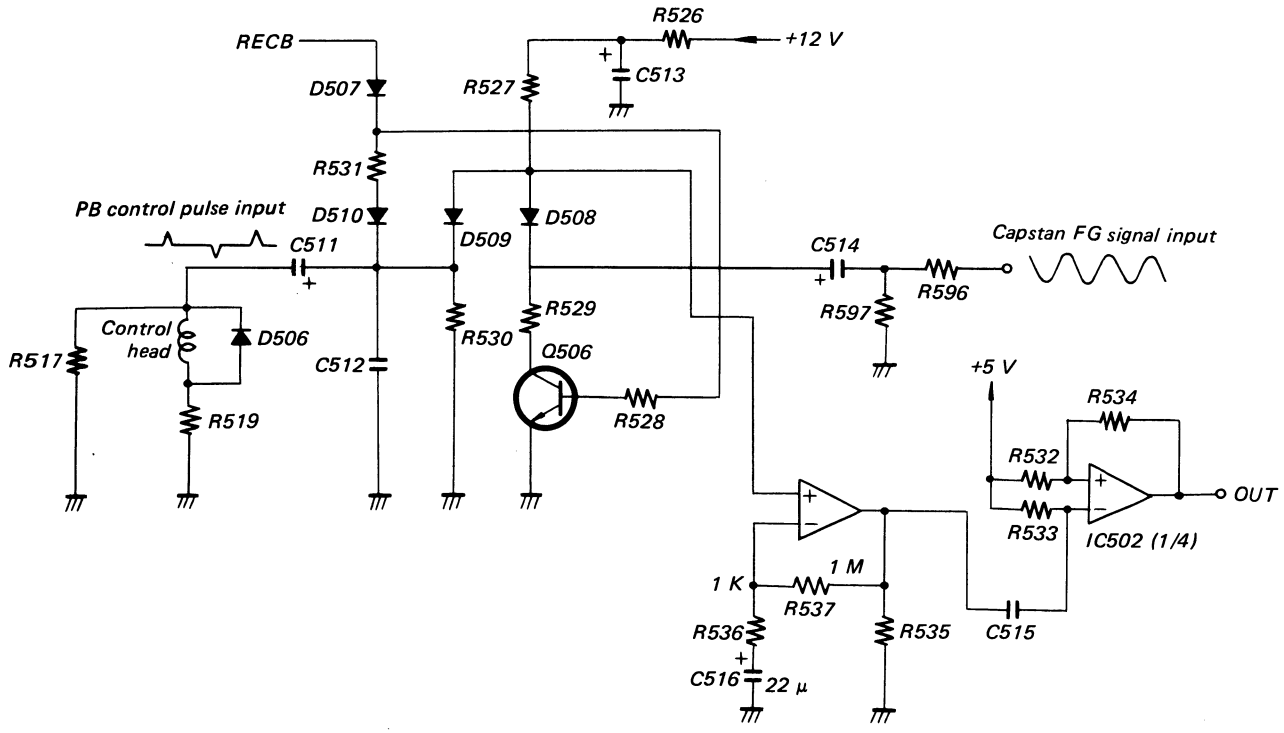



**Fig. 2-34 Recording Capstan FG Signal Processing, Playback Control Pulse Amplifier, Waveform Shaping, and Switching Circuits**

First, the operation of the above-mentioned circuit in the recording mode will be described. In playback, the recording +B line voltage is connected to the anode of D507. This turns Q506 on. A current flows through D507, R531, D510, and R530. This develops a voltage at the cathode of D509. Another current flows through R526, R527, D508, R529, and Q506, resulting in a voltage at the anode of D508. The values of the above-mentioned components are selected so that the former voltage can be higher than the latter. This means that D509 is cut off. The capstan FG signal fed through C514, therefore, changes the cathode voltage of D508. The result is that the anode voltage also is varied. The voltage input as the DC to the first operational amplifier stage in IC502 is determined in terms of R526, R527, D508, and R529. The input voltage has ripples suppressed appropriately. To the DC voltage is superimposed the FG signal, which is amplified about 60 dB. A series of R536 and C516 is placed to set the DC gain of the operational amplifier to unity (1) so that the operational amplifier may not be affected by the offset voltage, but its AC gain can be increased. The resistor R535 is placed to provide a resistance load for the operational amplifier so that its output waveform cannot be distorted.

The voltage divider, consisting of R596 and R597, prevents too high input capstan FG signal from being clipped to nonsymmetric waveform. If such a clipped, nonsymmetric waveform is passed through C515, the threshold level of the succeeding Schmitt trigger stage in IC502 deviates out of the vicinity of the time base for the sine wave. The result is that a change of the FG signal amplitude enters into the APC detector as an error, which causes wow and flutter.

The input, amplified FG signal is shaped to square wave, which is fed out.

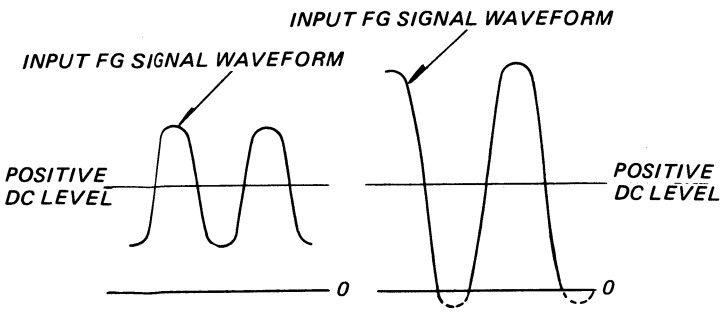



**Fig. 2-35 Operational Amplifier Outputs for Proper Input FG Signal (Left) and Too High Input FG Signal (Right)**

In turn, the control pulse in the playback mode of operation will be described in the this and following paragraphs. In playback, the recording B+ line voltage is not connected to the circuit (see Fig. 2-34. Therefore, Q506 is off and no current flows into D508. This means that the capstan FG signal cannot be led to the operational amplifier.

Current flows from the +12 V line through R526, R527, D509, and R530. This applies an reverse bias to D510. The control pulse input through C511 moves the cathode potential of D509. This fluctuates, or pulsates, the level at the positive input end of the first operational amplifier stage in IC502. AS the pulsating AC component at the positive input end is too low, care may not be taken in clipping as in the FG signal waveform. The operation of the operational amplifier in IC502 is similar to that in recording. The output of the operational amplifier is further magnified through the Schmitt circuit (FG signal amplifier ciruit shown in Fig. 2-37, the output of which enters pin 24 on IC501.

The FG signal from the capstan motor is led through shielded wire as in Fig. 2-37. The connection voltage of R547 and R548 is selected slightly lower than the turn-on level for the base of Q510. The coming FG signal is superimposed onto the connection voltage to switch on Q510. The output of Q510 is connected to pin 22 on IC501, which frequency divides the output FG pulse depending on the βformat, βII or βIII Format.

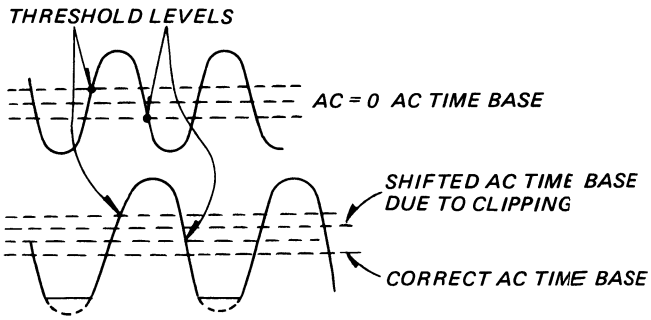



**Fig. 2-36 Schmitt Trigger Threshold Levels**

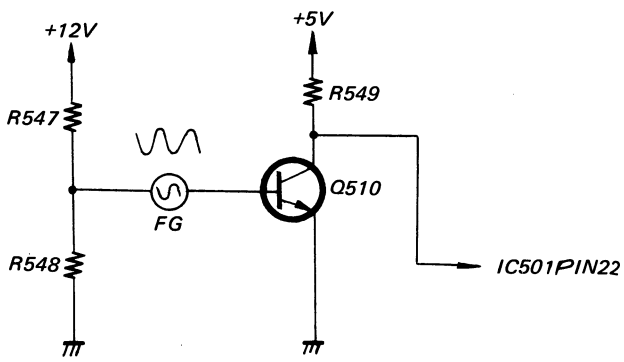



**Fig. 2-37 FG Signal Amplifier Circuit**

**(2) Phase Comparator, Speed Detector, and Frequency Divider Circuits**

All of the phase comparator, speed detector, and frequency divider circuits, which are housed in IC501, operate in digital fashions. The phase comparator circuit has the same timing relationship with the trapezoidal wave as that of the head APC described in Section 2-1-2-(2). In playback, however, tracking of the video heads must be done by delaying the phase of the control head in reference to those of the video heads. It is therefore needed that the delay time must be changed by forming a trapezoidal wave for the capstan in reference to a time lagged behind the start instant of the reference trapezoidal wave for the head APC.

The speed detector circuit operates in a way that the interval of the trailing edges of the FG pulses is measured. At the second clock of 895 kHz after the trailing edge of the FG pulse came in, the speed detector circuit starts forming a trapezoidal wave having such a time relationship as in Fig. 2-38. The first read pulse coming after the trailing edge of the FG pulse allows storing the position on the slope of the trapezoidal wave. The speed detector circuit produces a duty wave of pulse in proportion to the voltage at position. The duty wave is used as the AFC detection voltage.

The frequency circuits divide the frequencies of the recording capstan FG pulse and motor FG pulse to switch the tape speed dpending on the tape recording format, βII or βIII. Also, they change the frequencies for the double speed playback. Refer to Fig. 2-31. In the capstan control loop, the recording tape speed is determined almost by the capstan rpm which is govern by.

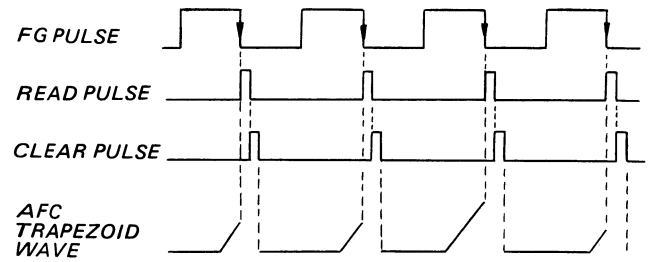
$$\frac{30\ \text{Hz} \times \text{frequency divisor}}{\text{Number of capstan FG teeth}}$$

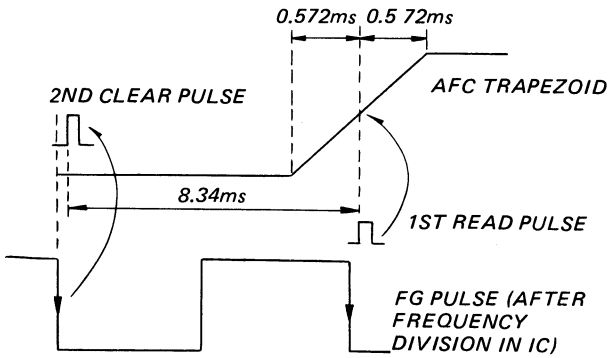
where the 30 Hz frequency is of the APC reference trapezoidal wave, if the APC is licked. The diameter of the capstan is determined so that the specified tape speed can be obtained when the capstan revolves at the above-mentioned revolutional frequency. In the AFC loop, on the other hand, the capstan motor will revolve at the frequency given by

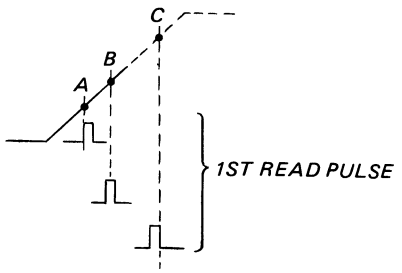
$$\frac{(120\ \text{Hz} \pm 7.2\%) \times \text{frequency divisor}}{\text{Number of motor FG teeth}}$$

where the frequency of 120 Hz ± 7.2% is of the AFC trapezoidal frequency, if the AFC is locked. The capstan motor and capstan, thus, revolve at the frequencies determined in the APC and AFC locking ranges. The pulley ratio, therefore, can be selected so as to satisfy the ratio of the two frequencies.

The motor FG pulse frequency division is made by the frequency divider in IC501 and the recording capstan FG pulse frequency division by Q507 through Q509. In recording, the motor FG pulse frequency division is switched to 1/3 or 1/2 according as the recording tape format is βII or βIII, determining the motor rpm. In the capstan FG pulse circuit, the interval of the trailing edges of the pulses coming into pin 24 on IC501 as the tachometer signal for the APC action is 33.3 msec at all times if the APC is licked. The period of the capstan FG pulse is substantially determined in terms of the motor FG pulse period and pulley ratio. For frequency division, therefore, a monostable multivibrator is used which provides a so-called "dead time" property that a single pulse is taken out every three pulses in the βII Format or every two pulses in the βIII Format, the other pulses being ignored. Also, see Fig. 2-39, the "Recording APC time Chart".



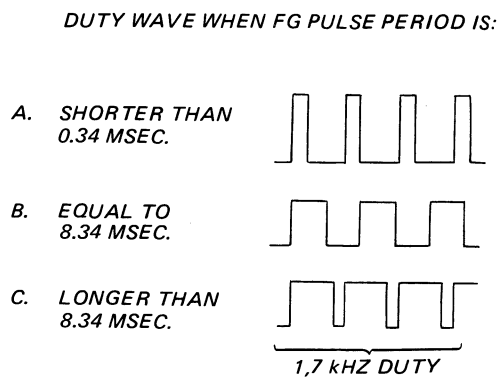




**Fig. 2-38 Principles of AFC Action**

The capstan FG pulse is input to, amplified, and waveform-shaped by IC502. It, then, is differentiated by C517 and R539. The resulted positive-going pulse triggers the succeeding stage of monostable multivibrator, consisting of Q509 and Q507. At the instant when it is triggered, Q507 is turned and holds on for approximately 26 msec of time determined by R544 and C518. The transistor holds on for the duration no matter how many pulses come in. When the duration elapses, Q507 turns off and is triggered by the succeeding positive-going pulse to turn and holds on again. The collector voltage of Q507, thus, is synchronized at the trailing edge with the FG pulse every three times for the βII Format or every two times for the βIII Format. The synchronized collector voltage is connected to pin 21 on IC501 for use as the tachometer pulse for the APC action. Note that in recording, Q508 is on and D551 provides no service.

In playback, the control pulse induced from the tape, instead of the capstan FG pulse, is amplified by IC502 and turn Q508 off. It, also, passes R540 and D511 and enters pin 24 on IC501 for use as the tack pulse for the APC action. Note that as the +B line is disconnected from Q507, D513 provides no service.

**(3) Tracking Circuit**

In recording, also the pulse input to pin 24 on IC501 is used for the APC action as described previously. IC501, therefore, operates in the playback mode either when the VTR is in the recording or playback mode of operation. Accordingly, the level at pin 23 should be low. A change of the tracking time constants of C533, R506, or R553 or the TRACKING knob on the front panel, however, causes the APC reference trapezoidal wave phase to move transiently during recording. The result is that the APC action is disturbed. To prevent such a disturbance, Q525 is turned on during recording so that the APC action can maintained even by turning the TRACKING knob at least. Note that during recording, the APC reference trapezoidal wave phase is not in relation with the switching pulse.

In recording, the control pulse is put on the tape in a phase relationship as in Fig. 2-33. The distance between the video heads over the tape and control head position and video head installation height. As the video head width is 27 μm and the track interval 30 μm for the βII Format or 20 μm for the βIII Format. however, recording is overlapped by 3 μm in the βIII Format as illustrated in Fig. 2-40. The result is that the center of each recording video head deviates 3/2 μm from that of the recording track even if the same recorded tape is played back with use of the same VTR unit. In playback, therefore, the phase of each video head, or the switching position, must be somewhat led in reference to that of the control pulse.

6P Particular VTR units can be different in the distance between the control pulse on the tape and corresponding video track. The capstan APC reference trapezoidal wave phase can be deviated from the head APC reference trapezoidal wave phase can be deviated from the head APC reference trapezoidal wave phase so as to provide an optimum tracking performance. Refer to Fig. 2-41-(a) the "Playback APC Time Chart".

An experiment shows that in the βIII Format, the switching pulse may be led approximately 0.5 msec in advance of the control pulse. The shaped control pulse is 0.5 msec in advance of the playback control puse. The switching pulse and shaped control pulse are adjusted in phase by the tracking delay signal. As recording is not overlapped on the tape in the βII Format, the phase difference of the playback control pulse from the switching pulse may be equal to the one in recording, or approximately 0.5 msec, and tracking is not shifted in switching the βII Format to the βIII Format and vice versa.

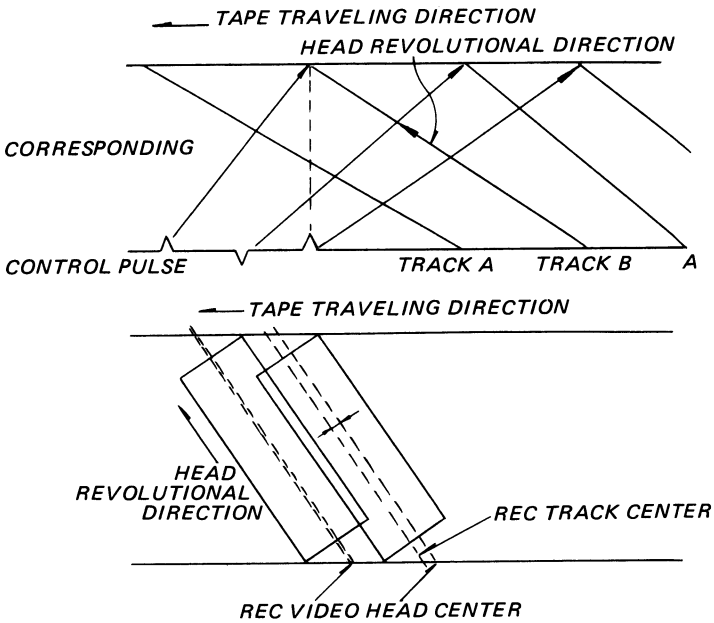



**Fig. 2-40 Corresponding of Recording Control Pulse and Recording Video Signal (Upper) and Deviation of Recording Video Head Center from Recording Track Center by Overlapping Recording (Lower)**

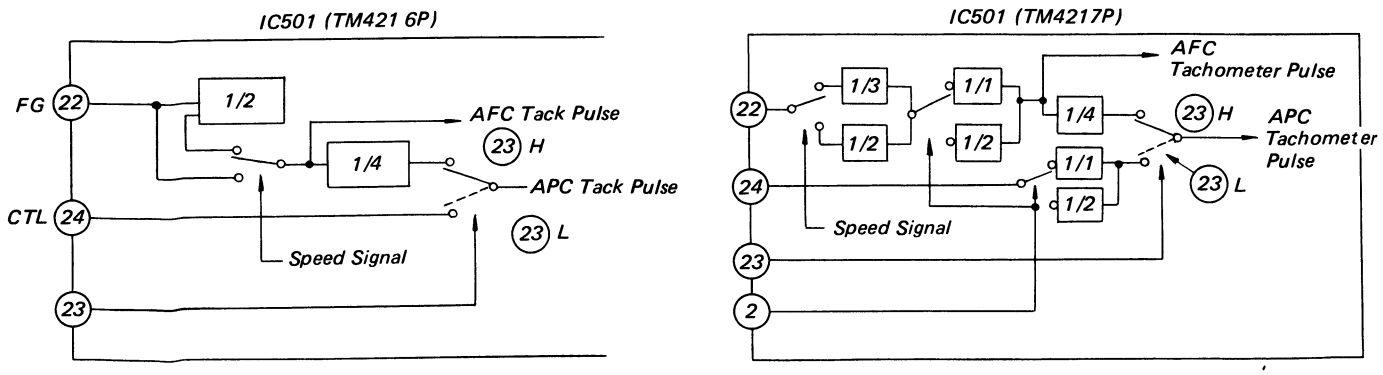
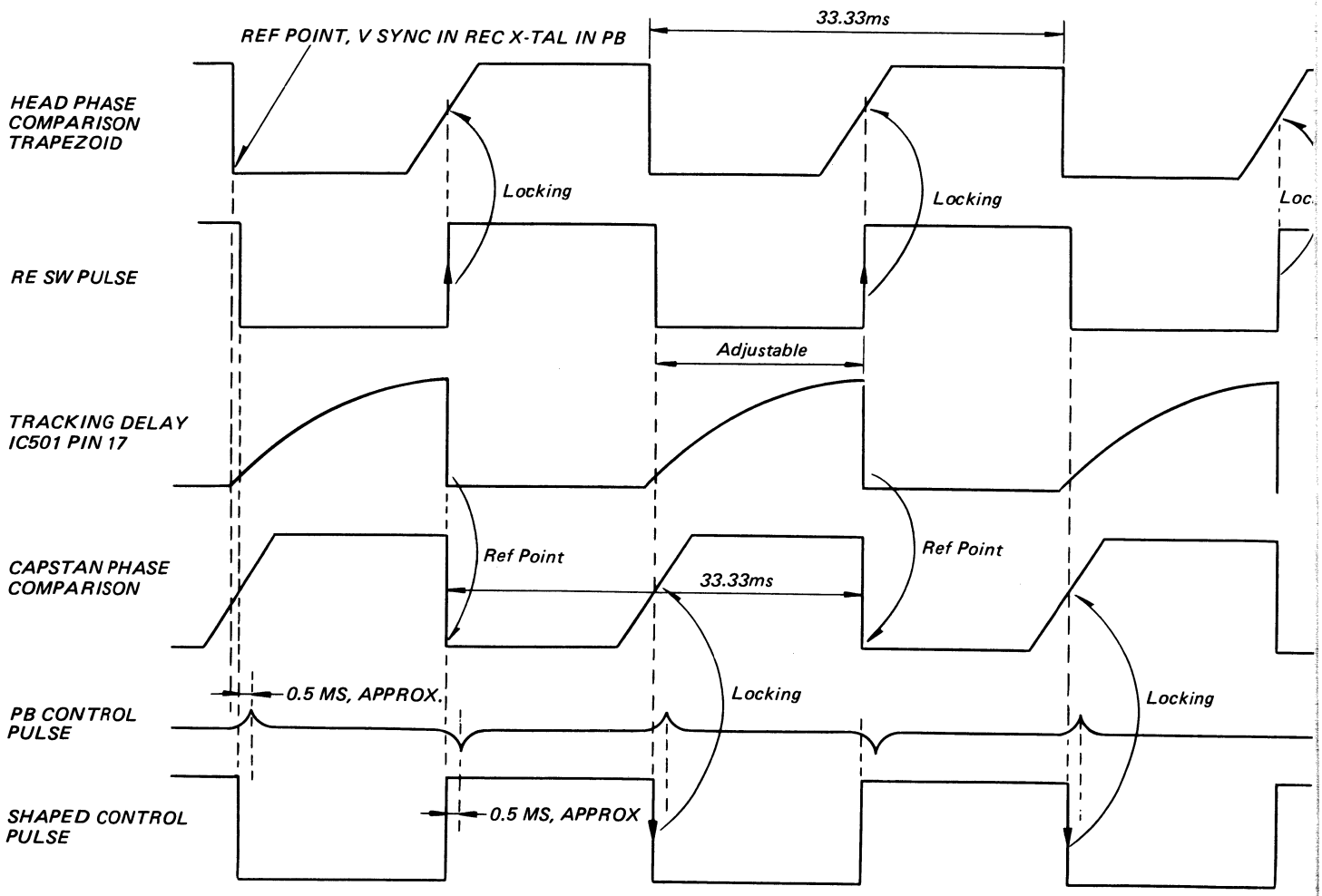
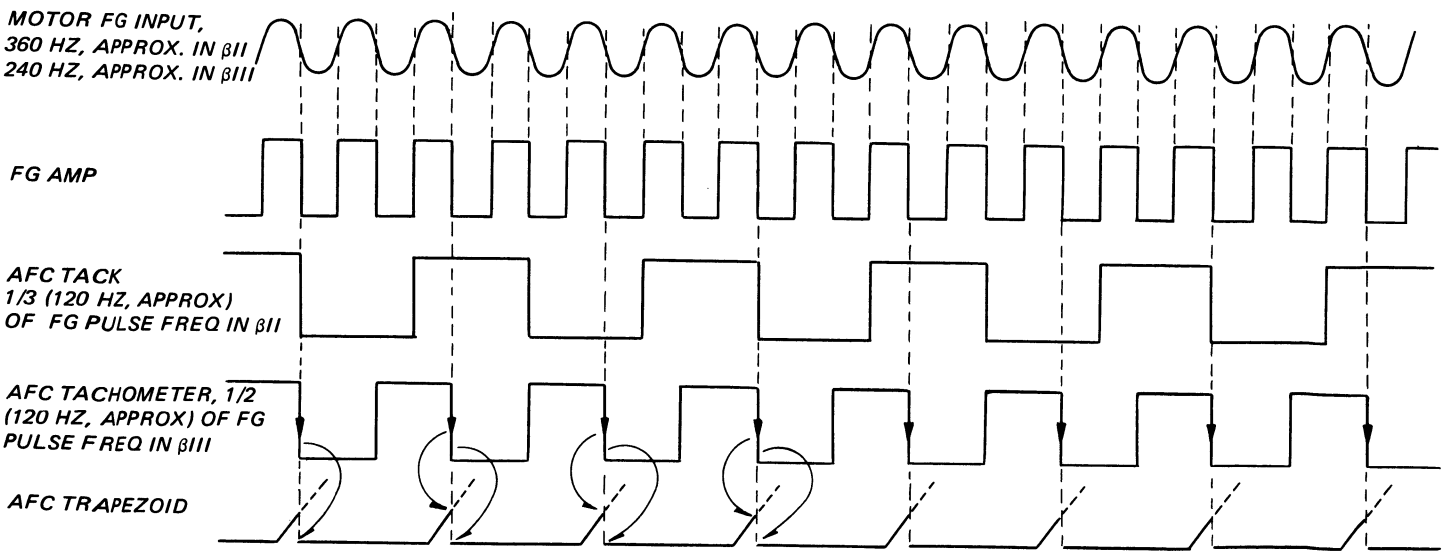



**Fig. 2-39 Capstan FG Pulse/Control Pulse Input Switching Circuit**




(a) Playback APC Time Chart




(b) Recording and Playback AFC Time Chart

**Fig. 2-41 Playback APC Time Chart and Recording and Playback AFC Time Chart**

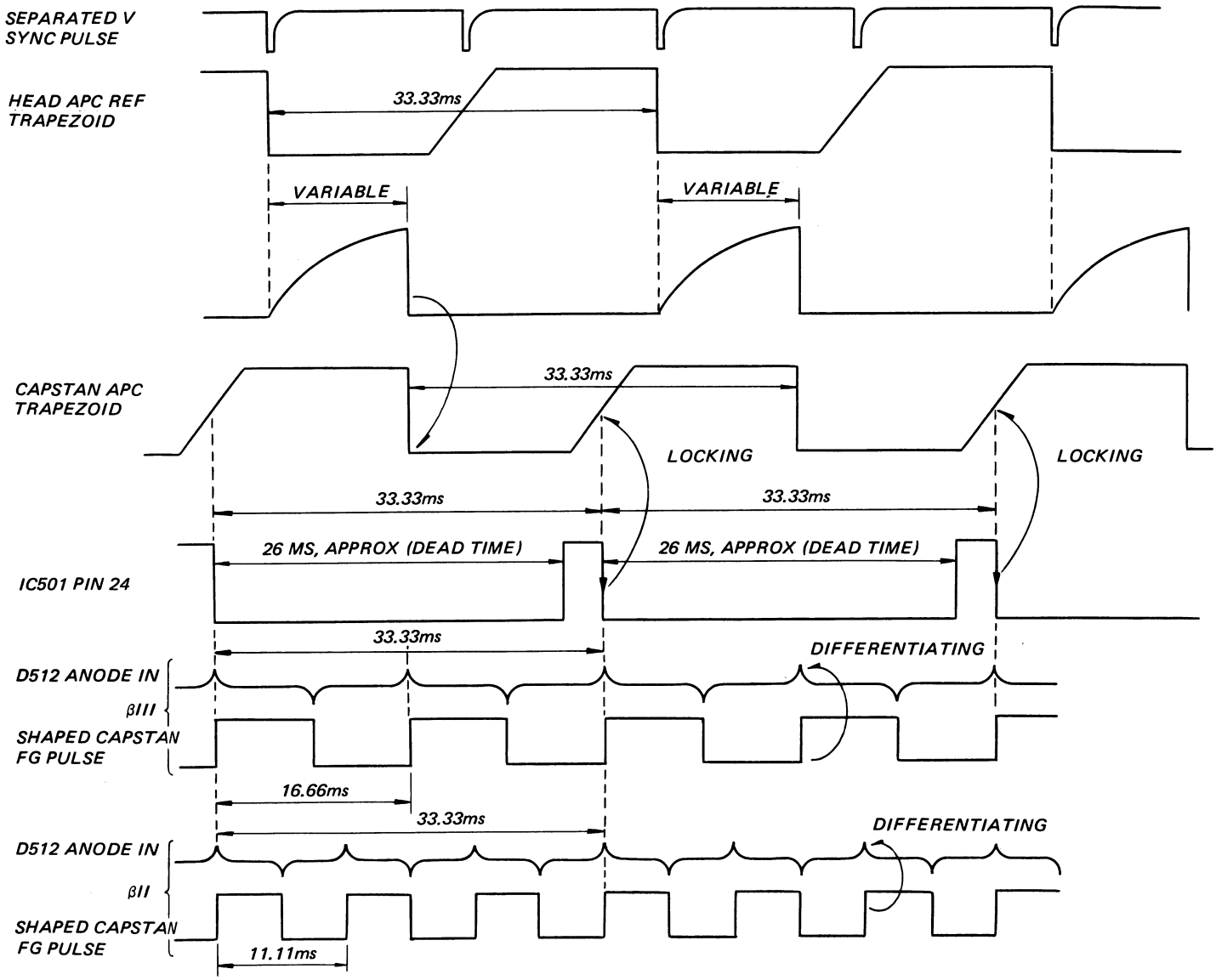



**Fig. 2-42 Recording APC Time Chart**

**(4) Phase Compensation and Capstan Motor Drive Circuits**

The detected APC and AFC signals are fed out of pins 7 and 8 on IC501, respectively. The output signals are combined as will be described below. The added signal has the carrier eliminated, passes the phase compensation filter, and is compared with the reference voltage at pin 9 on IC502. The difference voltage drives the push-pull drive circuit, consisting of Q512 and Q513, which revolves the capstan motor.

The APC and AFC signals are added up, through their respective resistors in a proper proportion. The added voltage enters pin 10 on IV502 and as described in the head servo control section, balances with the one at the negative end, pin 9. The APC output at pin 7 on IC501 may considerably change because of the compensation for the wow and flutter of the tape running. The duty cycle, therefore, should be locked at 50%, or at the center on the slope of the trapezoidal wave. The smoothed voltage at that time may be approximately 2.5 V. A division of the voltage so added with that of the smoothed AFC voltage. The sum becomes equal to the voltage at pin 9 on IC502 for servo action.

Accordingly, a ratio of the two above-mentioned divisions may be decided to determine the transmission ratio of the motor to the capstan. In recording, this in turn determines the capstan revolutional frequency, the motor revolutional APC output voltage, which is licked at the slope of the APC trapezoidal wave so that it can be equal to the one at pin 9 on IC502.

In playback, similarly, the transmission ratio sequentially determines the capstan revolutional frequency so that the control pulse frequency can be 30 Hz, the motor revolutional frequency, the AFC output voltage, and finally the APC output voltage. This determines the position of the control pulse to be locked on the slope of the APC trapezoidal wave. The phase relationship with the switching pulse is adjusted by the tracking delay signal as described previously.

Stopping of the capstan motor is done by the disk motor turn-off signal delivered from D539. The capstan motor is stopped only in the still state, but keeps revolving in the fast-forward, rewinding, or picture search mode of operation.

The reason that the resistance of R569 is selected high is to prevent the potential at the negative end of C522 from decreasing too low when the VTR is stopped, that is, to assure that the motor can revolve at any time when the stop state is released. The reason for the connection of R565 to the +B line is that when power is turned on, current is charged into C522 to raise the voltage at pin 10 on IC502 for starting the motor. The feedback network of C523, C524, and R570 placed from the motor output to the operational amplifier eliminates the 1.7 kHz carrier and raise the DC loop gain. C524 is nonpolarized electrolytic capacitor as a reverse bias is applied to it.

### 2-1-4 Recording Tape Speed Switching and Playback Tape Speed Auto-switching Circuits

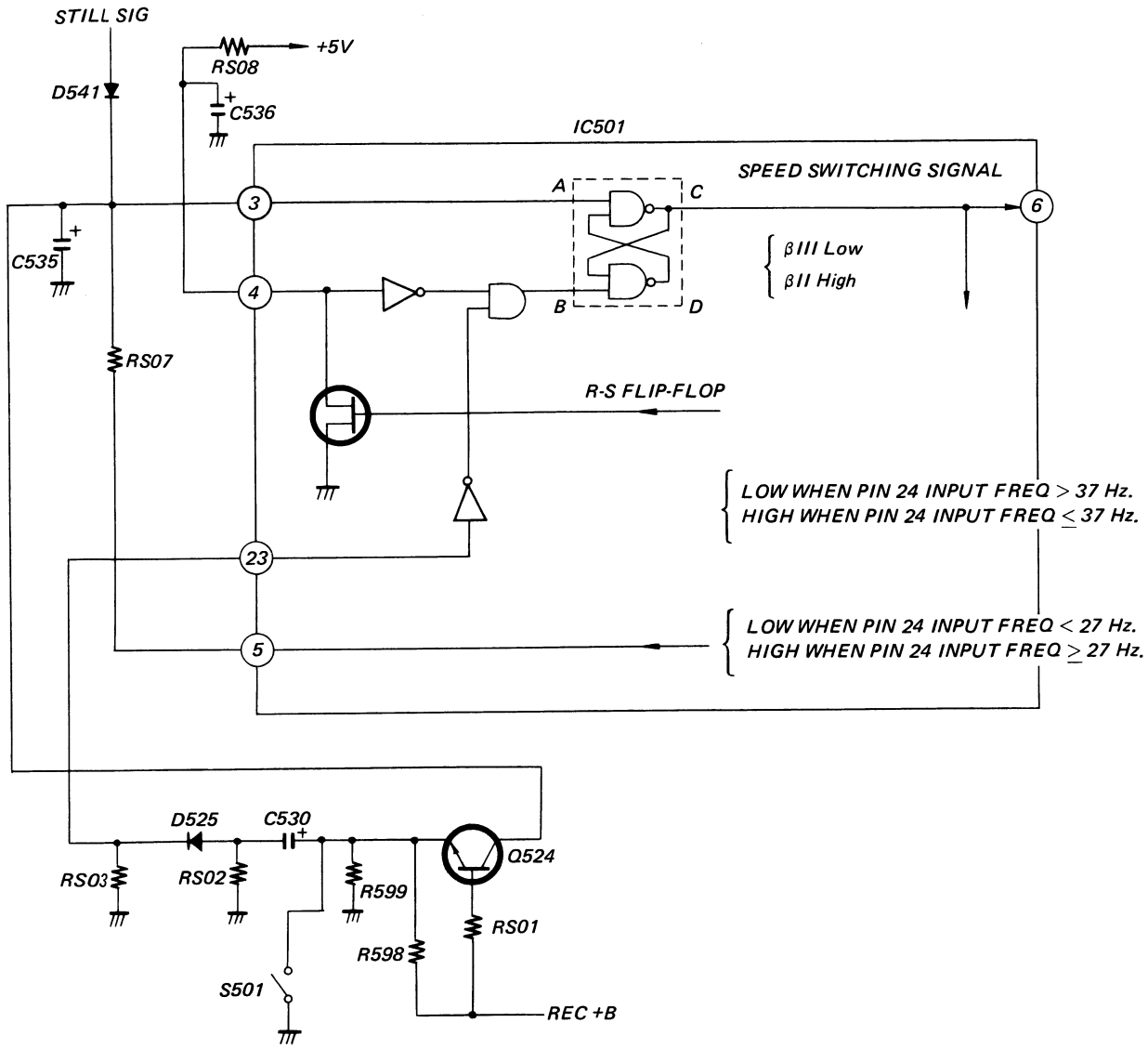
In recording, the tape speed is switched by the βII/III selector switch on the front panel in the way that a speed signal changes the frequency division of the capstan motor FG pulse. In playback, the frequency of the control pulse is detected to make a second speed signal, which changes the frequency division. The following describes the tape speed operation in more detail.

In recording, as mentioned previously, IC501 is operated in the playback mode. The voltage at pin 23 on IC501, therefore, must be made zero. For the purpose, an external circuit is used as in Fig. 2-43, being described below.

A. For a tape speed set by the βII/III selector switch before recording is started,
   - A-1 When S501 is closed,
     Pin 5 is low.
     Pin 23 is low (case III).
   - A-2 When S501 is open,
     Pin 3 is high.
     Pin 23 has a positive-going pulse (case I).

B. For a tape speed set by the βII/III selector switch during recording,
   - B-1 When S501 is turned from open to close,
     Pin 3 is low.
     Pin 23 is low (case III).
   - B-2 When S501 is turned from close to open,
     Pin 3 is high.
     Pin 23 has a positive-going pulse (case I).

In either case A or B, the speed signal for the βIII Format is issued when S501 is open and the speed signal for the βII Format is given when it is closed.




| CASE | I | II | III | IV |
|---|---|---|---|---|
| A | I | O | O | I |
| B | O | O | I | I |
| C | O | I | I | PRECEDING STATE HELD |
| D | I | I | O | |
| REC MODE | βIII | βII | βII | |

State of R-S flip-flop in IC501

**Fig. 2-43 Tape Speed Switching Circuit**

The level at pin 23 on IC501, as mentioned above, is normally made low. A narrow, positive-going pulse is used to set or reset the R-S flip-flop. The pulse prompts the IC to be momentarily made in the recording mode of operation; but, this does not affect the tape speed switching operation.

The tape recorded in the βII Format may be played back at the speed for the βIII Format. The result is that lower control pulse frequency is detected. The tape recorded in the βIII Format, on the contrary, may be played back at the speed for the βII Format. The result is that higher control pulse frequency is detected. The detected control pulse frequency prompts the flip-flop to produce a speed signal, which switches the frequency division of the FG pulse. If the tape recorder in the βII Format is played back in the βIII Format, for example, pin 5 is low, pin 3 low, the input A low, and the input B high, that is, the flip-flop state is in the case III. The flip-flop emits the speed signal for the βII Format. The input frequency at pin 24 becomes 30 Hz. Consequently, the flip-flop becomes settled in the case IV. The diode D541 is placed to raise the level at pin 3 to the high level in the playback still state. The high level retains the mode of operation, right before the still state, set by the high level at the pin B by the control pulse lower than 27 Hz at pin 24. This allows the capstan motor to quickly start at the time when the still state is released.

### 2-1-5 Muting and Trick Play Signal Generator Circuit

As the video muting signal is detected either of the control pulse at pin 5 on IC501 or the head servo unlock signal at pin 12 on IC501. The video muting signal is high when is delivered to the Video Circuit to mute upon no video signal portions or for servo unlock. The audio mute signal is obtained in the way that the video mute signal and special playback signal are input to the OR gate. The audio mute signal output of the OR gate is delivered to the Audio Circuit. The special playback signal is routed to the Video Circuit where it is used for forming a false sync pulse, DOC-off signal, and others.

### 2-1-6 High-Speed Picture Search (Super Scanning) Circuit

In the picture search mode of operation, the tape is run at a high speed as the reel table is driven by the disk motor. As seen from Fig. 2-44, the number of horizontal scanning lines for a single field in rewinding playback is more than 262.5 in regular playback and the one in fast-forward playback is less than 262.5. It is seen that the relationship between the disk motor rpm and tape speed is determined in terms of the transmission ratio of the disk motor to the reel and the tape winding diameter. The tape speed, thus, changes depending on the current tape winding diameter. The result is that the angle of the video track to the head track changes, or the number of horizontal scanning lines changes as much as that of one field at the end of winding. This means that the playback horizontal scanning frequency changes so that the horizontal scanning cannot be synchronized and a normal picture cannot be obtained.

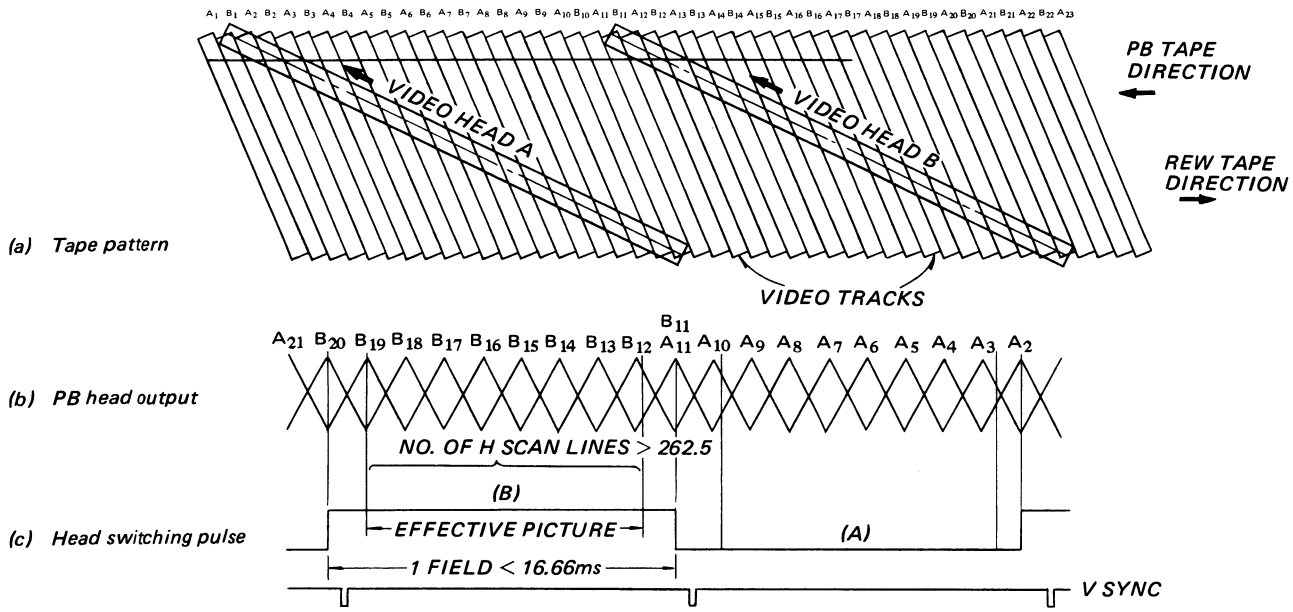
To solve such a distrubance problem, there is used an automatic cylinder speed control loop which detects the playback horizontal scanning frequency. If this is lower than 15.734 kHz, the loop increases the cylinder speed or if higher, it slows down the speed, thereby keeping the playback horizontal line, frequency at 15.734 kHz.

For example, consider that in rewinding playback, the playback horizontal scanning frequency is lower than 15.734 kHz when the video head traces on track B in Fig. 2-45. The loop can detect the low frequency to accelerate the disk motor speed. This, also, makes the tape run faster, shortening the period of tracing a single field. The result is that the video head is moved so as to trace on track A. The number of horizontal scanning lines increases slightly more than that of track B. This means that the time required for tracing a single field, or the time required for a half turn of the disk motor, per the number of horizontal scanning lines in the single field can be made rather short period. In other words, the playback horizontal scanning frequency can be increased. If it is raised too high, the reverse action is taken and consequently, the playback horizontal scanning frequency is settled to the present value of 15.734 kHz.

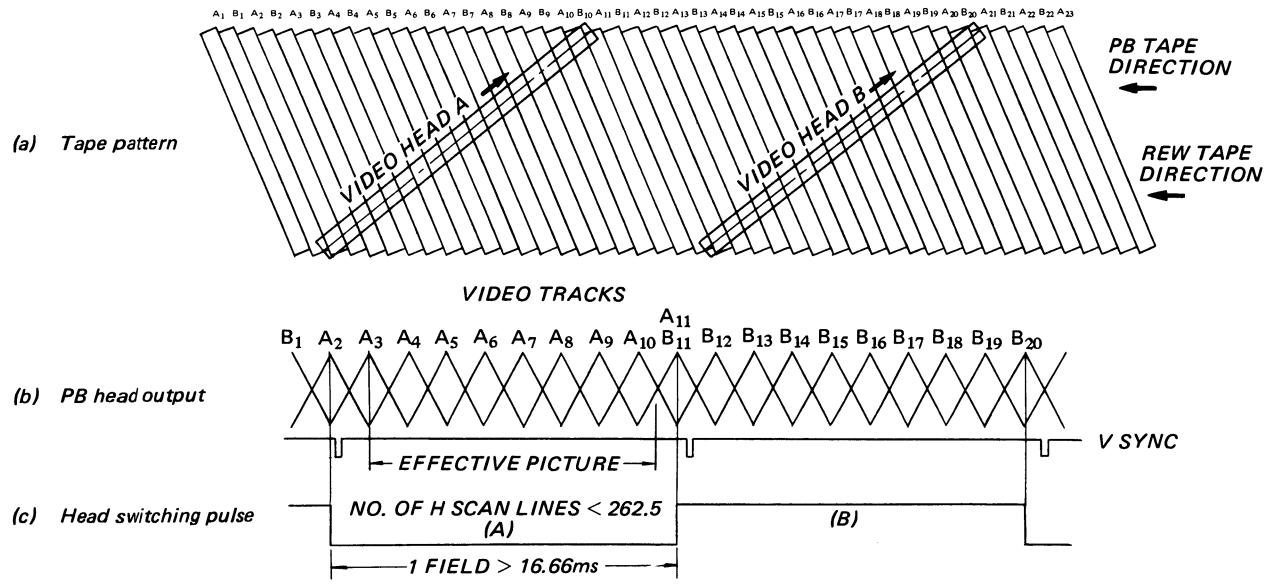
Also, the automatic cylinder speed control loop can compensate the horizontal scanning frequency for a change due to the variation of the tape speed depending on the amount of tape wound.

Further, the automatic cylinder speed control loop provides a more positive advantage that the transmission ratio of the motor to the tape is switched so as to maintain stable picture without no horizontal scanning line disturbance when the tape is run a different speed. For illustrating this, you may consider an analogy that in Fig. 2-45, trace B corresponds to the trace for a lower transmission ratio and trace A to the trace for a higher. When the disk motor is revolved at the same rpm, there may be a large difference between the two head trace gradients. The gradient difference can be somewhat reduced by the above-mentioned horizontal scanning compensation. Note that the present super scanning circuit provides the edition feature of horizontal lines only in the $\beta$III Format playback mode of operation where horizontal alignment is made.

This and the following paragraphs describes the operation of the super scanning circuit in more detail with reference to the block diagram in Fig. 2-24. The cylinder tape traveling circuit, as described previously, is formed as a closed loop with respect to the horizontal scanning frequency. It, also, can be said a kind of AFC closed loop in the sense that the horizontal scanning frequency is detected and a voltage corresponding to the frequency is fed out. For the reason, the playback horizontal sync pulse is given from the Video Circuit and is amplified by Q531. The amplified pulse triggers the succeeding T flip-flop, consisting of Q532 and Q533, which produces a square wave having 50% duty cycle and a half of the pulse frequency. The square wave passes RS62 and C542 and the LC resonant circuit, consisting of L501, C545, and the like, is turned to resonance at its fundamental frequency. D528, then, has a sine wave at the cathode. One end of the Lc resonant circuit is fixed to the potential determined in terms of R554. The negative envelope of the sine wave is detected by D528, RS36, and C546. The LC resonant circuit can be designed to be turned to resonance at a predetermined frequency. This allows a resonant voltage to be obtained depending on the input frequency. The resonant voltage is detected. The detected voltage which is in proportion to the input frequency is connected through the buffer transistor Q534 to the operational amplifier as the disk motor phase differential amplifier in IC502, in regular playback with the input from pin 13 on IC501 disconnected by D531. The amplified voltage drives the disk motor.




a. Rewinding tape pattern and playback output




b. Fast-forward tape pattern and playback output

**Fig. 2-44 Head Tracks, Playback Output Envelope, and Switching Pulse Phase in Picture Search**

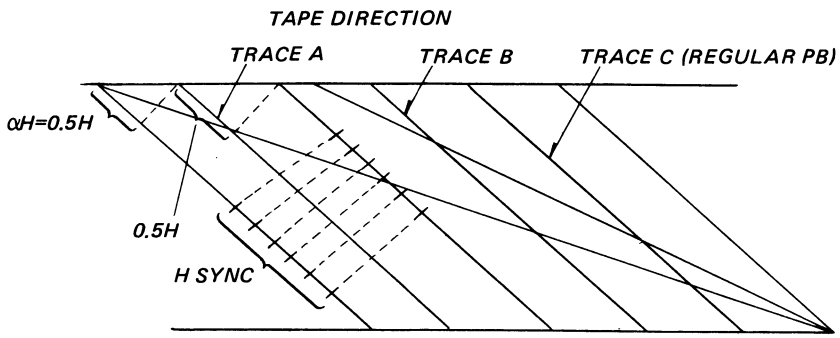



**Fig. 2-45 Head Traces by Different Tape Speed in Rewinding Playback in βIII Format**

The operational amplifier, which has an infinite DC gain as Q535 is turned off, balances with the detected voltage becoming equal to the voltage at pin 6 on IC502, the latter voltage being determined in terms of R584. The horizontal scanning frequency at the balancing voltage can be adjusted to 15.734 kHz by level-shifting the detected voltage with R554.
The transistor Q536 is turned off to disconnect the highpass filter, consisting of R587 and C527, to make stable the automatic cylinder speed control loop. Q538 is turned on to charge the voltage of the same phase as in the ordinary playback into C526 and C525 so that a good transient response can be obtained when the picture search is switched to the playback mode. D534 conducts only in the regular ordinary playback mode.
An effect of C544 is as follows. The pair of video heads can have lacks of the signal picked up from the tape. From such no-signal portions the horizontal sync pulse cannot be obtained. This does not allow the flip-flop, consisting of Q532 and Q533, to function, causing sine wave resonant voltage to fluctuate tranciently. The result is that the transient voltage drives the disk motor as an error voltage. The time constant of RS36 and C546 is taken longer to maintain the resonant voltage to abrupt drop and C544 keeps it against sudden rise, thus preventing noise bars from affecting the detected voltage.
As seen from the resonant curve in Fig. 2-46, the control effect is reversed at frequencies higher than the resonant frequency. The loop results in oscillation in the vicinity of point B. This may happen in such cases that either fast-forward or rewinding is switched over to the picture search and the high-speed search is suddenly switched over to the low-speed search. When there are no signals, it cannot be known what horizontal signal is input.
The motor, therefore, can be stopped by noises at frequencies near the resonant frequency.
To prevent such failure, the super scanning circuit includes a detector circuit, consisting of Q541 through Q545. The operation is illustrated in Fig. 2-47. The period of the high level at the base of Q544 is longer than that of the low level when the input frequency is out of a range around of the horizontal sync frequency. The high level pulse is integrated. If the input frequency is not proper, the integrated signal turns Q545 on to disconnect the picture search signal, or the cue and review signal. This suppress the head revolutional frequency to the ordinary playback rpm of 30 Hz so that it can be locked by the switching pulse, thereby preventing picture disturbance. For noises or no signal input, proper differentiation by C549 and RS51 is not obtained. This holds the base level of Q544 high, which disconnects the picture search signal.
The reason for use of the LC resonant detecting circuit for the picture search is that it has a temperature drift characteristic superior to similar analog detecting circuits.
In the picture search mode, only the AFC loop is provided, but the head phase control is not made. The head switching position may deviate a little depending on the cylinder revolutional frequency if the recording and playback phases are correct. Such a deviation does not raise a problem as the resulted switching noise, however, can be hidden far out of the effective picture area.

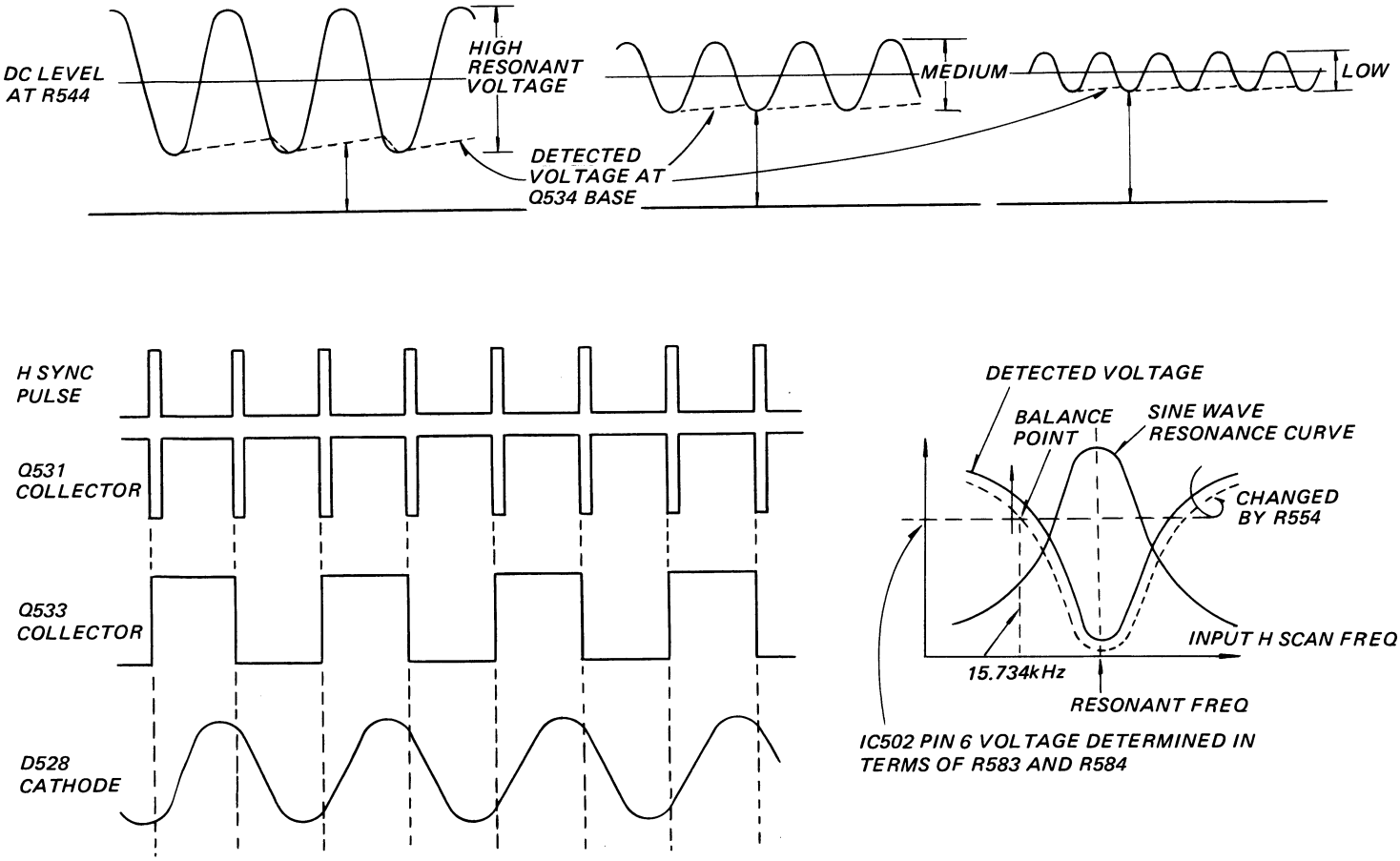



**Fig. 2-46 Resonant Voltage Change, Detected Voltage, and Time Chart**

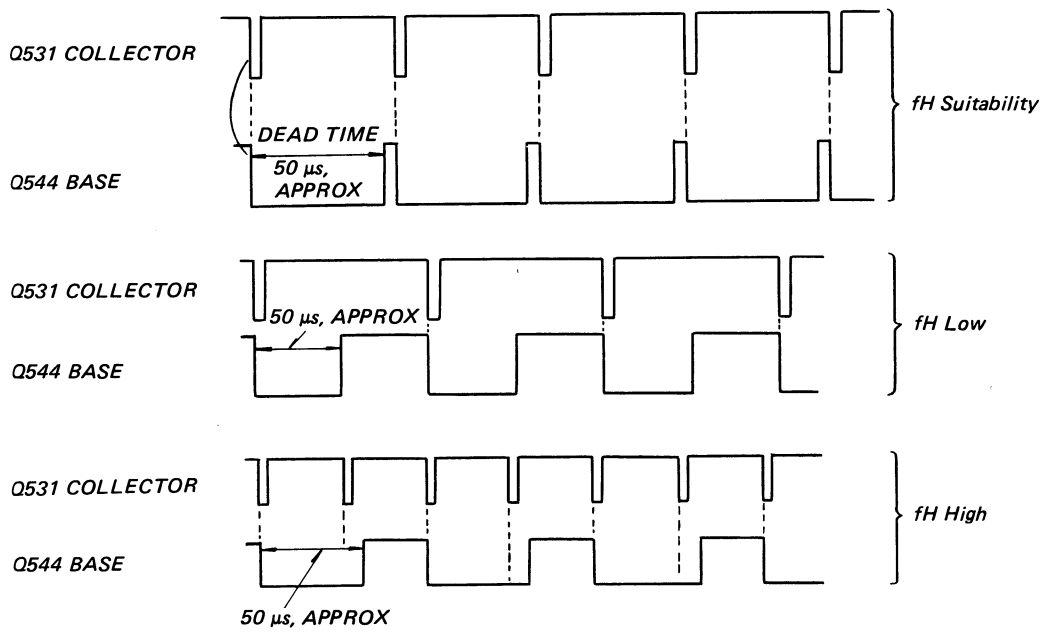



**Fig. 2-47 Miss Lock Detector**

### 2-1-7 Double-Speed Circuit

For double-speed playback, the divided frequencies of the capstan control signal and FG signal are further halved to revolve the capstan as high as two times. Switching of the frequency division is done by making low the level at pin 2 on IC501. The low-level signal is delivered to the Logic Circuit.

In the double-speed playback, both APC and AFC in the capstan servo circuit are locked. Noises are shifted into the vertical blanking by tacking adjustment. As seen in Fig. 2-48, there are two tracking shift directions. They should be corrected with the X2 TRACKING control so that tracking can be shifted in either direction.

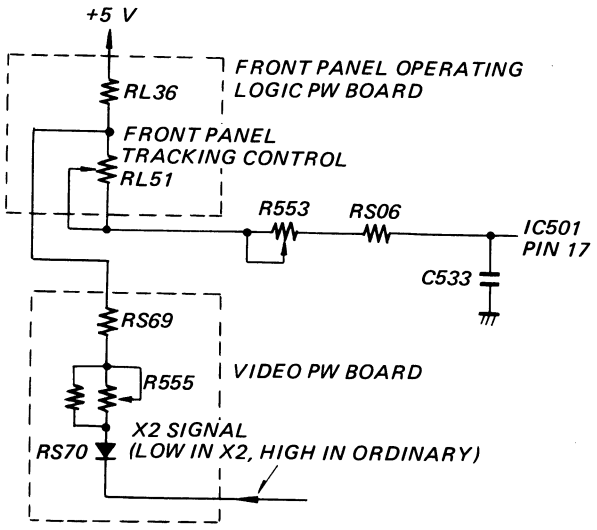



**Fig. 2-49 Double Speed Tracking Shift Circuit.**

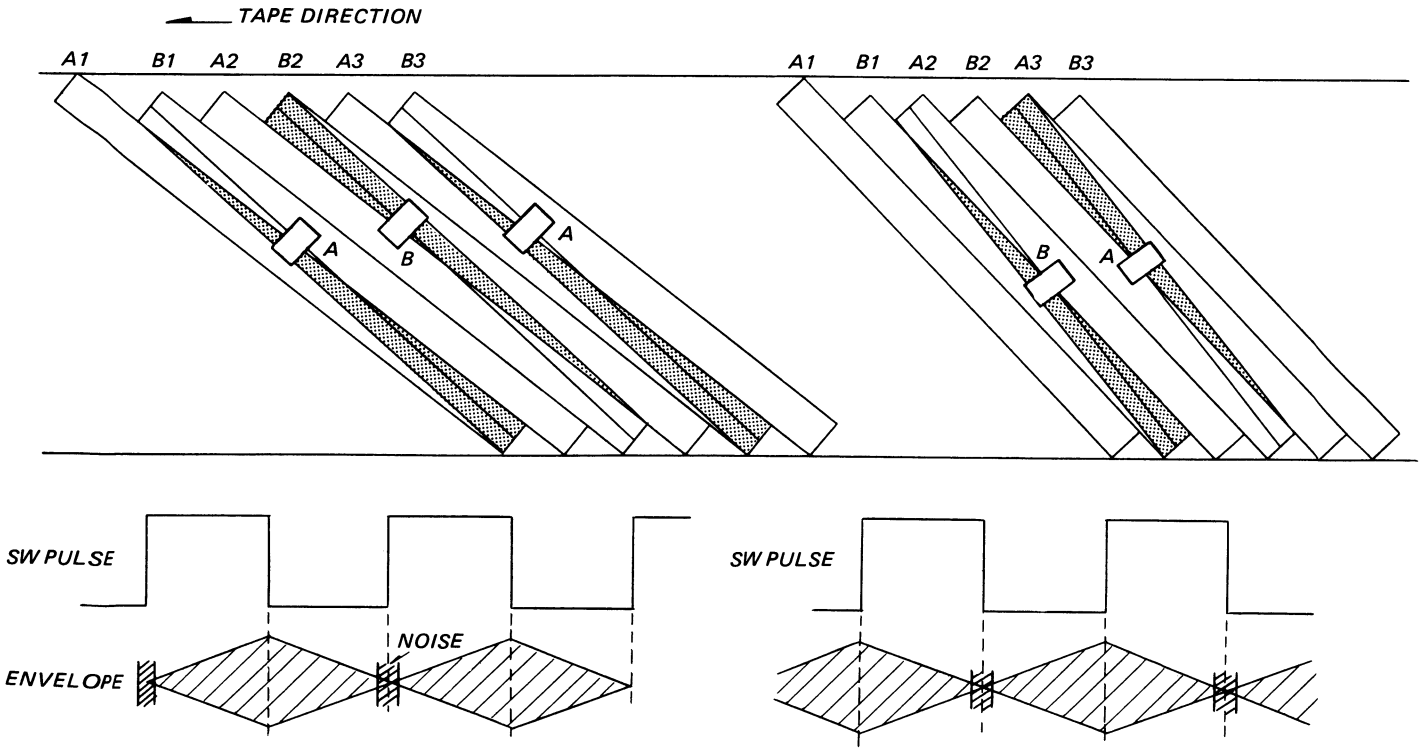



**Fig. 2-48 Two Cases of Head Trace for Double Speed Playback**

## 2-2 LOGIC CONTROL SYSTEM

### 2-2-1 Introduction

The Logic Control System consists of a System Control Control Circuit board PW2233 containing a microcomputer TMP4320P, a Front Control Circuit board PW2235 having inputs of setting a desired mode of operation, and a Solenoid Drive Circuit board PW2350 for energizing functional plunger solenoids.

The System Control Circuit where the single-chip 4-bit micro-computer TMP4320P functions as the heart outputs motor on-off signals, plunger solenoid on-off signals, LED (light-emitting diode) on-off signals, and power on-off signals for each mode of operation. These on-off features provide direct mode switching that is impossible by conventional logic control mechanisms.

A single hybrid in the Logic Control System houses a variety of sensor circuits, thereby reducing the number of component parts used. In addition, a new timing adjustment circuit is provided, which prevents playback picture noises which were seen at pause spliced points in recording edition by usual models.

### 2-2-2 Construction

Fig. 2-50 is a block diagram for the Logic Control System, including the System Control Circuit, Front Control Circuit, and Solenoid Drive Circuit.

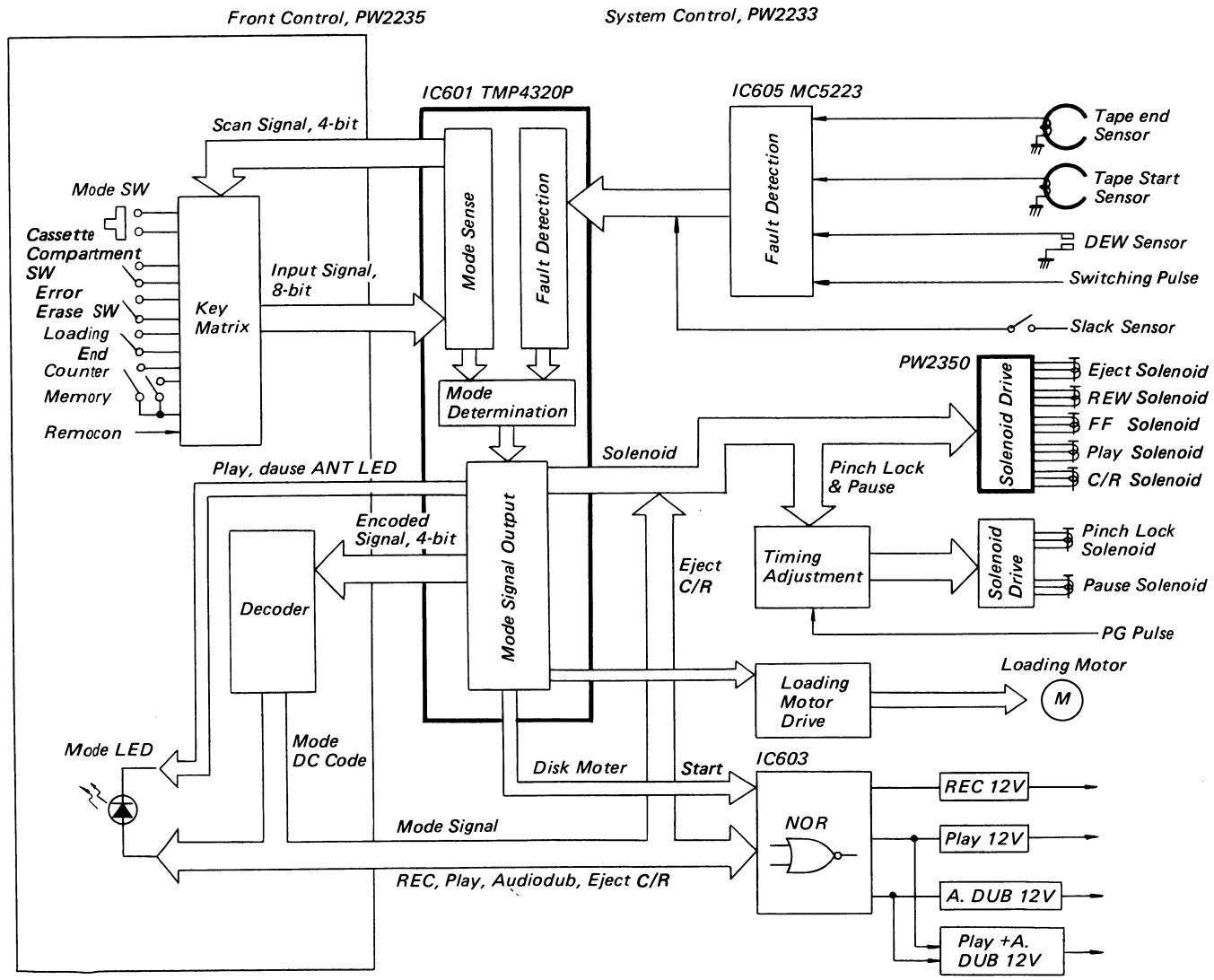



**Fig. 2-50 Logic Control System Block Diagram**

### 2-2-3 Description of Major ICs

#### TMP4320P (IC601)

**1. General**

TMP4320P, which is a single-chip 4-bit microcomputer fabricated in a N-CH MOS process, has a ROM of 8 bits by 2048, a RAM of 4 bits by 128, 3 input ports of 12 bits, 4 output ports of 15 bits, and 2 input/output ports of 8 bits. The IC is housed in plastic DIP package, which has 42 pins as shown in Fig. 2-51. The IC provides such major functions as to input the signals from the operating key switches, sensors, and microswitches, to determine the mode, to determine whether the mode switching can be accepted or not, and to issue ignals for driving corresponding plunger solenoids, illuminating corresponding LEDs, starting or stopping the motors, and others. For more detail, see Table 2-2.

Table 2-2 TMP4320 (IC601) Pin Input and Output Sygnals and Logic Levels

| Pin No. | Input or Output | Description |
|---|---|---|
| 1 | – | TEST (NC) |
| 2 | – | |
| 3 | IN | LOW input when disk motor is not revolving. |
| 4 | – | |
| 5 | IN | LOW input when dew develops or tape slacks. |
| 6 | OUT | LOW output when play solenoid is energized. |
| 7 | OUT | LOW output when rewind solenoid is energized. |
| 8 | OUT | LOW output when fast-forward solenoid is energized. |
| 9 | OUT | LOW output when pinch lock solenoid is energized. |
| 10 | OUT | LOW output when pause solenoid is energized. |
| 11 | – | |
| 12 | OUT | LOW output when PLAY LED is lit. |
| 13 | OUT | LOW output when PAUSE LED is lit. |
| 14 | – | |
| 15 | – | |
| 16 | OUT | LOW output when ANTENNA indicator is in VCR. |
| 17 | OUT | LOW output when disk motor is revolving. Also, used to turn heater off when it is revolving. |
| 18 | – | |
| 19 | OUT | LOW output when loading motor is in loading. |
| 20 | OUT | LOW output loading motor is in unloading. |
| 21 | | Ground |
| 22 | – | INT (NC) |

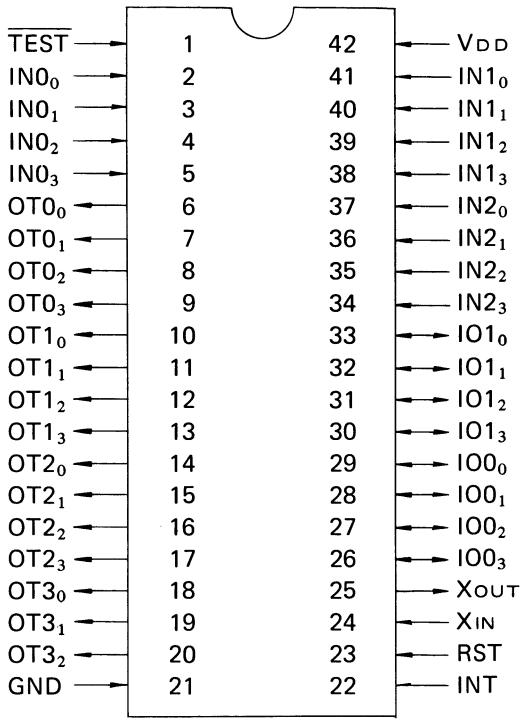



**Fig. 2-51 TMP4320 Pin Configulation**

| Pin No. | Input or Output | Description |
|---|---|---|
| 23 | IN | RESET, or RESET with LOW input. |
| 24 | | Clock from 455 kHz ceramic oscillator. |
| 25 | | |
| 26 | | Encoded mode signal outputs (see Table 2–10). |
| 27 | | |
| 28 | | |
| 29 | | |
| 30 | OUT | Scan 4 output |
| 31 | OUT | Scan 3 output |
| 32 | OUT | Scan 2 output |
| 33 | OUT | Scan 1 output |
| 34 | IN | Input 8 |
| 35 | IN | Input 7 |
| 36 | IN | Input 6 |
| 37 | IN | Input 5 |
| 38 | IN | Input 4 |
| 39 | IN | Input 3 |
| 40 | IN | Input 2 |
| 41 | IN | Input 1 |
| 42 | | VDD, 5 V |

NOTES: The HIGH level is 5 V and the LOW level 0 V. The dash (–) indicates that the pin is not connected (NC).

Tablr 2-3 Output of IC601 (Micro Computer)

| PIN NO. | MODE / OUTPUT | LOAD-ING | EJECT | REW | STOP | FF | AUDIO DUB | AUDIO DUB PAUSE | REC | REC PAUSE | RE-VIEW | PLAY | STILL | CUE | X2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 6 | PLAY SOL | | | | | | ○ | ○ | ○ | ○ | | ○ | ○ | | ○ |
| 7 | REW SOL | | | ○ | | | | | | | ○ | | | | |
| 8 | FWD SOL | | | | | ○ | | | | | | | | ○ | |
| 9 | PINCH LOCK SOL | | | | | | ○ | | ○ | | | ○ | ○ | | ○ |
| 10 | PHASE SOL | | | | | | | ○ | | ○ | | | | | |
| 12 | PLAY | | | | | | | | | | | ○ | ○ | | |
| 13 | PAUSE | | | | | | | ○ | | ○ | | | ○ | | |
| 16 | ANT | | | | | | ○ | ○ | | | ○ | ○ | ○ | ○ | ○ |
| 17 | DISK MOTOR | | | ○ | | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| 19 | LOADING M. + | ○ | | | | | | | | | | | | | |
| 20 | LOADING M. − | | ○ | | | | | | | | | | | | |
| 26 | DECODER A | | ○ | | | ○ | ○ | ○ | | | ○ | | | | |
| 27 | DECODER B | | ○ | ○ | | | | | ○ | ○ | ○ | | | | ○ |
| 28 | DECODER C | | ○ | ○ | | ○ | | | | | ○ | | ○ | | ○ |
| 29 | DECODER D | | ○ | ○ | | ○ | ○ | ○ | ○ | ○ | | | ○ | ○ | |

* ○ → LOW LEVEL

## 2. Internal Functions

(1) Automatic rewinding: When the end of the tape running in a forward direction as in the playback, recording, or similar mode of operation is detected with the AUTO REW switch turned on, the VCR is automatically set to the rewinding mode. In the timer-controlled recording, the automatic rewinding cannot be done.

(2) Counter memory: When the tape counter reaches "9-9-9-9" in the rewinding mode of operation with the COUNTER MEMORY switch turned on, the VCR is set to the STOP state.

(3) Automatic TV-VCR Switching: When the VCR is switched to the playback, audio dubbing, cue, review, or double speed mode of operation, it is automatically set for use of the VCR. By depressing the TV-VCR selector pushswitch in and out, either of the VCR or TV is selected cyclically for operation.

(4) Timer-controlled recording: The timer output signal sets the VCR in the recording mode with the REC INH switch turned off. In the timer-controlled recording, all the key input and remote control signals except the TV-VCR selector cannot be accepted. The automatic rewinding cannot be done even if the AUTO REW switch is turned on.

(5) Camera pause: The camera pause signal, if coming from the TV Camera during the recording mode, sets the VCR into the recording pause mode. If it is disconnected, the VCR is reset to the recording mode. The signal is not effective in the timer-controlled recording.

(6) Automatic pause resetting: Any of the recording pause, audio dubbing pause, and still mode is reset in approximately 6 min 30 sec since the VCR was halted. Note that in the camera pause, it is switched over to the stop state.

(7) Loading motor protection: In the event tape loading operation continues longer than 12 sec, the VCR is automatically switched over to unloading operation. If unloading takes longer than 20 sec, also, it is automatically stopped. These preventive operations are needed to protect the loading motor against too high load.

(8) Disk motor protection: A faulty stop of the disk motor automatically switches the VCR over to the stop state. This switching feature does not function until approximately 8 sec elapse after the start of the disk motor. If in the timer-controlled recording the disk motor will not start with the feature doing three times of action, the VCR is switched over to the stop state.

(9) Dew and tape slack prevention: If the low dew or tape slack signal comes in, this prompts any mode of operation to be switched over to the stop state. The low signal prevents any of the operating key signals and remote control signals except the EJECT key signal from being accepted until the low signal goes off. If the VCR is in tape loading operation, the low signal switches it over to unloading operation.

(10) Record safety: If the REC INH switch is on, the record safety feature inhibits any mode of operation from being switched over to the recording or audio dubbing mode.

(11) Tape end detection: If the end of tape is detected in a forward mode of operation such as playback or if the beginning is detected in a reverse mode of operation such as rewinding or review, then any mode is switched over to the stop state. In such a tape end detection in the forward mode of operation with the AUTO REW switch turned on, however, it is switched over to the rewinding mode. Also note that in the timer-controlled recording, the tape cannot be automatically rewound.

(12) Tape sticking prevention: When tape loading ends or the fast-forward, rewinding, cue, or review mode of operation is switched over to the stop mode, the play solenoid is energized to actuate the tension lever to slacken the tape. When the playback, recording, or audio dubbing mode of operation is switched over to the stop state, the tension lever is released to slacken the tape.

(13) Automatic backet lifting: If a tape cassette is not in the backet with the cassette detect switch held off, the backet is automatically lifted up when power is turned on. Note that if the tape cassette is in the backet, the tape is loaded.

(14) Remote control inputs: The 4-bit binary-coded remote control signal from PL04 is accepted at the time when the strobe is low. The signal is decoded in the microcomputer for remote control. Table 2-4 shows a remote control code.

Table 2-4 Remote Contol Code

| MODE | D | C | B | A |
|---|---|---|---|---|
| – | L | L | L | L |
| STOP | L | L | L | H |
| CUE | L | L | H | L |
| REVIEW | L | L | H | H |
| – | L | H | L | L |
| – | L | H | L | H |
| PLAY | L | H | H | L |
| Double Speed | L | H | H | H |
| – | H | L | L | L |
| STILL | H | L | L | H |
| – | H | L | H | L |
| – | H | L | H | H |
| – | H | H | L | L |
| – | H | H | L | H |
| – | H | H | .H | L |
| – | H | H | H | H |

**NOTE:** A remote control key has priority to any key except the PAUSE key on the VCR body when they are depressed at the same time.

### 3. Initialization

It is necessary to initialize the microcomputer so as to begin execution of the program from a certain address when power is turned on. This is made in the manner that the reset (active low) pin 23 on IC601 is set to the low level. A usual initializing circuit is an integrating network to which an additional diode is placed as illustrated in Fig. 2-52.

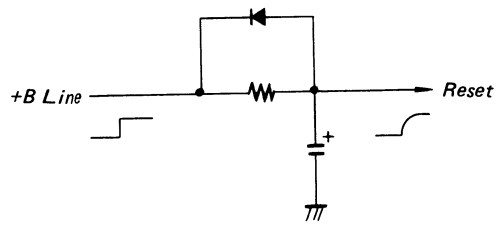



**Fig. 2-52 A Simple Initializing Network**

The initializing circuit used in the present Logic Control System provides a secure resetting upon a momentary service interruption as constructed in Fig. 2-53. The usual initializing network in Fig. 2-52 is not involved in any problem as long as the period of service interruption is rather long. Too short interruption can possibly cause the program to run away when the line becomes recovered with the voltage at the reset pin on the microcomputer being near the threshold level. In the present initializing circuit in Fig. 2-53, the decrease of the line voltage prompts the zener diode D605 to securely turn Q617 off, which turns Q618 on. This assures that the reset output goes down to the low level.

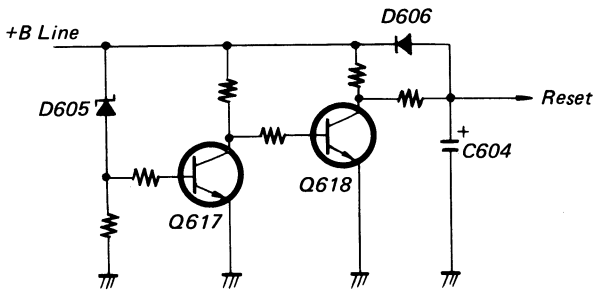



**Fig. 2-53 Initializing Circuit Used in Present Logic Control Circuit**

## 2-2-4 MC5223 (IC605)

### 1. General

MC5223 is a single-chip, 21-pin SIP hybrid IC having sensor and associated circuits. It provides tape end detections at the beginning and end of tape disk motor revolution detection, dew detection, and similar functions.

### 2. Circuit Operation

Fig. 2-54 shows MC5223 and associated circuits.

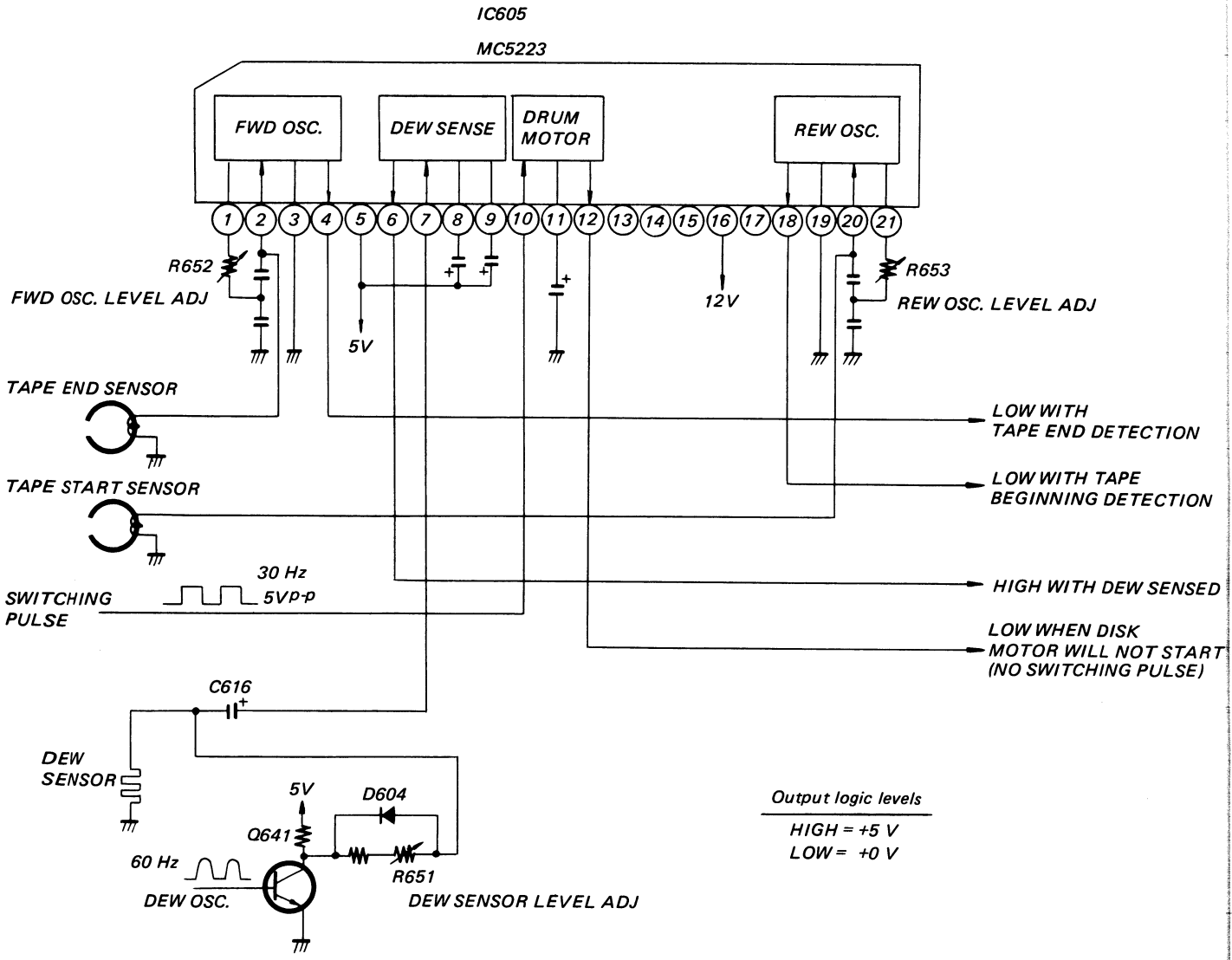



**Fig. 2-54 MC5223 and Associated Circuits**

(1) Tape end detector: The tape beginning detector and tape end detector circuits are the same in the construction. The tape end detection circuit having a forward sensor, therefore, is described below.
The tape end detector circuit, as shown in Fig. 2-55, is made up of a LC oscillator, consisting of Q4, inductance component of the tape sensor, and capacitor, When the metal foil attached to the end of tape comes close to the tape sensor, the Q of the tape sensor coil decreases. This stops the oscillation. The oscillation frequency $f$ is expressed by the relation.

$$f \doteqdot \frac{1}{2\pi\sqrt{LC}}$$

where $L$ is the inductance of the tape sensor coil and $C$ the serial capacitance of C605 and C606. Their respective selected values are 180 $\mu$H, 0.0039 $\mu$F and 0.022 $\mu$F. The oscillation frequency $f$, then, is approximately 200 kHz.
When the oscillation stops, Q5 is turned off, which turn Q6 on. The output at pin 4 goes to low. The low output indicates that the tape end has been detected.

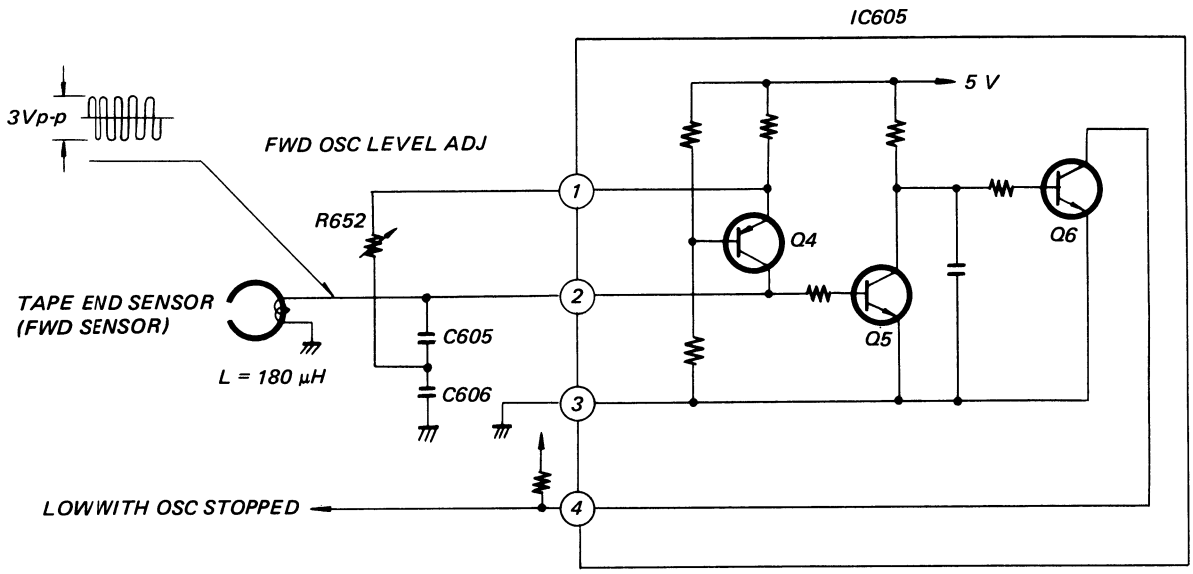



**Fig. 2-55 Tape End Detector Circuit**

(2) Dew detector: As shown in Fig. 2-56, a 60 Hz, 4 Vp-p to 6 Vp-p pulse is applied to pin 7 on IC605. If dew is sensed, the resistance component of the dew sensor decreases. The result is that the amplitude of the pulse becomes low. The low pulse is connected through Q11 to the Schmitt trigger circuit, consisting of Q12 and Q13. When dew is sensed, Q12 is turned off and Q13 on. This turns Q14 on, which makes the output at pin 6 high.

To reset the dew detection state, a reset pulse to be applied to pin 7 must have a hysteresis allowance higher than the pulse amplitude for dew detection. The reason is that Q12 and Q13 form the Schmitt trigger. Such a feature prevents a sort of oscillation that the dew detector circuit repeats detection and reset, when the pulse input is critical in the detection amplitude.

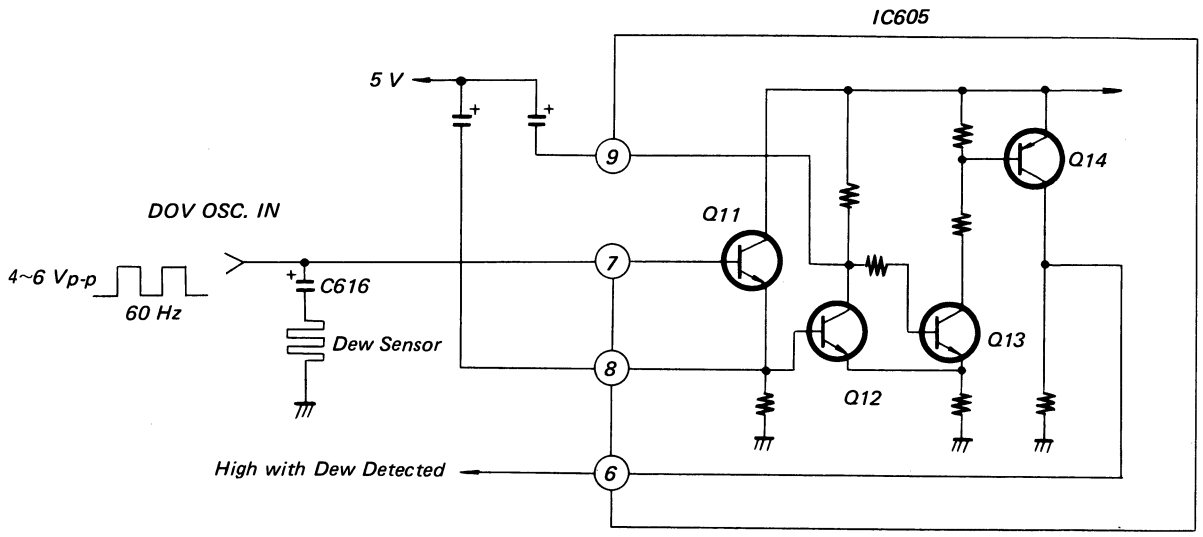



**Fig. 2-56 Dew Detector Circuit**

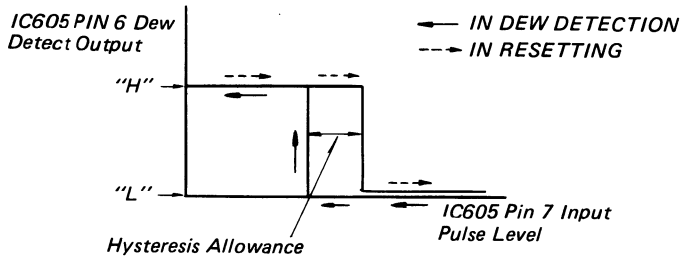



**Fig. 2-57 Dew Detection Hysteresis Characteristic**

(3) Disk motor revolution detector: This detects the revolution of the disk motor by the presence or absence of the switching pulse as illustrated in Fig. 2-58. If the switching pulse is present, Q16 is turned off. If it becomes absent, Q15 is turned off, which turns Q16 on. This makes the output at pin 12 go to the low level.

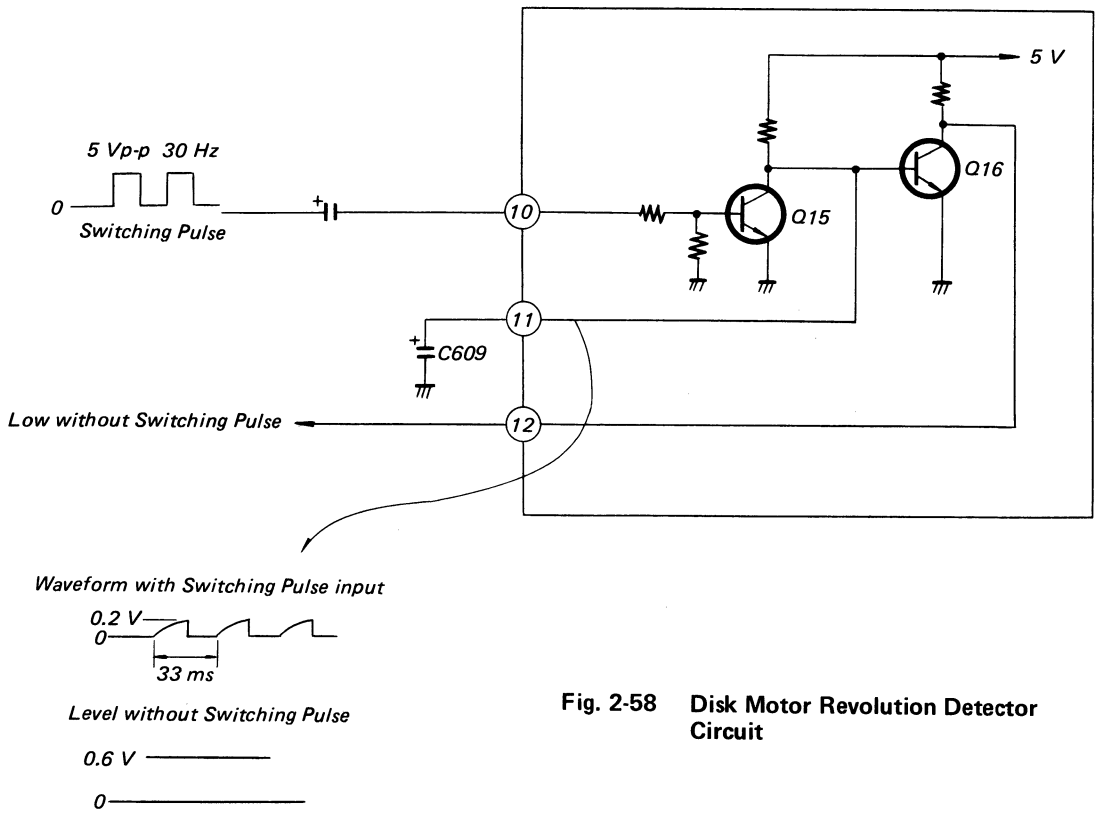



**Fig. 2-58 Disk Motor Revolution Detector Circuit**

### 2-2-5 Key Sensing Matrix

The signals from the operating keys may be input to the microcomputer one by one. This input method, however, is not appropriate for the microcomputer because of too much number of inputs. In the present logic Control Circuit, the number of inputs to the microcomputer is reduced in a multiprocessing of key signals that the 4 bit scan signals output of the microcomputer and 8 bit signals input to it are connected 4 by 8 in a matrix fashion. A depressed operating key can be known by the microcomputer in the way that the high-level one of the eight input signals is detected at the time when one of the four scanning signals is present (see Fig. 2-59).

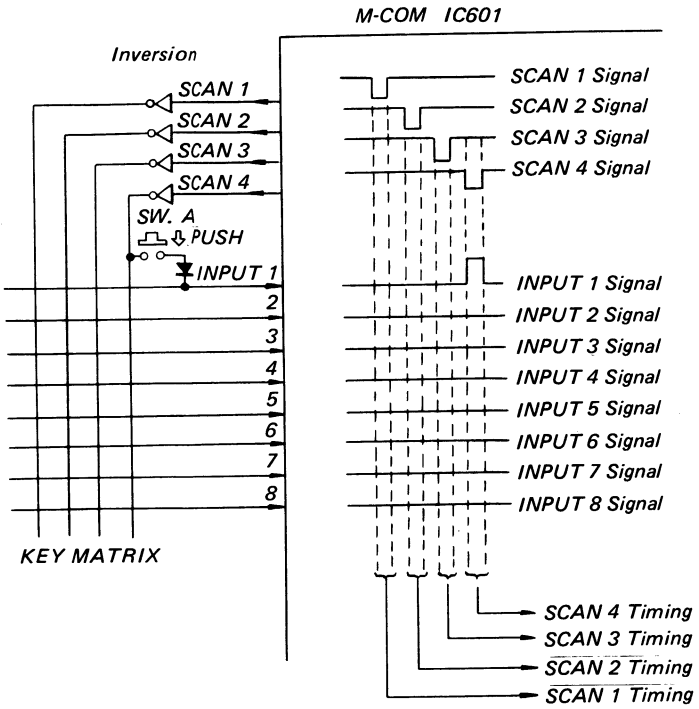


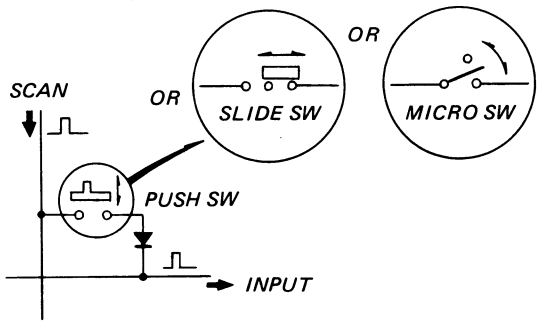

**Fig. 2-59 Key Sensing Matrix**

**NOTE:** If the switch A is depressed, for example, the input 1 signal goes to high at the time of the scanning 4 signal. The microcomputer, then, knows that the switch A was depressed.

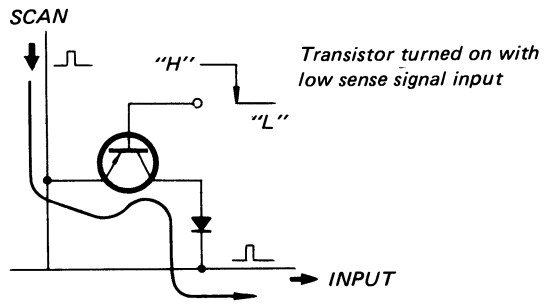
There are four types of devices for turning on or off the key sensing matrix scanning lines and input lines:

(1) Mechanical pushswitches, including the PLAY, REC, and other located on the front panel.
(2) Mechanical slide switches, including the AUTO REW switch SL15.
(3) Mechanical microswitches, including the cassette detect switch, recording INH switch, and others.
(4) Electronic switches, including the timer-controlled recording switch (QL21) and remote control input switch (QL16 through QL20).

Each of the electronic switches given in the last item (4) operates in the way, as illustrated in Fig. 2-60 (b), that the scanning signal is applied to the emitter of a PNP transistor and is allowed to flow through the collector when an active-low sense signal lowered the base potential enough to turns the transistor on.




**(a) Mechanical switch**




**(b) Electronic switch**

**Fig. 2-60 Switches Used in Key Sensing Matrix**

### 2-2-6 Mode Switching

Switching of the V-8000T from one present mode of operation over to another mode is different in the priority depending on the both modes. Tables 2-5 and 2-6 show mode switching possible for one another in the control by the VCR body and Remote Control unit, respectively. Table 2-7 is mode switching possible by multipressing function keys (buttons). It should be noted that the Remote Control unit can switch over from the still state to the playback mode also by depressing the PLAY button and can switch over form the audio dubbing pause state to the playback mode by depressing only the PLAY button, while the VCR body has to have the PAUSE/STILL button depressed to reset the pause or still state.

**Table 2-5 Possible Mode Switching on V-8000 VCR Body**

| Switching mode \ Preset mode | EJECT | REW | STOP | FF | PLAY | PAUSE | REC | AUDIO DUB | REVIEW | CUE |
|---|---|---|---|---|---|---|---|---|---|---|
| Only Cassette Holder Locked | ○ Backet up | X | X | X | X | X | X | X | X | X |
| In Loading | ○ Unloading | △ | △ | △ | △ | X | △ | △ | △ | △ |
| EJECT | | □ | □ | □ | □ | X | □ | □ | □ | □ |
| REW | ○ | | ○ | ○ | ○ | X | X | X | ○ | ○ |
| STOP | ○ | ○ | | ○ | ○ | X | ○ | ○ | ○ | ○ |
| FF | ○ | ○ | ○ | | ○ | X | X | X | ○ | ○ |
| PLAY | ○ | ○ | ○ | ○ | | ○ (Still) | ○ | ○ | ○ | ○ |
| STILL | ○ | ○ | ○ | ○ | X | ○ Pause reset) | ○ (Rec pause) | ○ (Dub pause) | ○ | ○ |
| REC | ○ | X | ○ | X | X (Note 1) | ○ (Rec pause) | | X | X | X |
| REC PAUSE | ○ | X | ○ | X | X | ○ (Pause reset) | X | X | X | X |
| AUDIO DUB | ○ | ○ | ○ | ○ | ○ | ○ (Audio dub pause) | ○ | | ○ | ○ |
| AUDIO DUB PAUSE | ○ | ○ | ○ | ○ | ○ (Still) | ○ (Pause reset) | ○ (Rec pause) | X | ○ | ○ |
| REVIEW | ○ | ○ | ○ | ○ | ○ (Note 2) | X | X | X | | ○ |
| CUE | ○ | ○ | ○ | ○ | ○ | X | X | X | ○ | |

○ Direct switching possible.
△ Switching after end of loading.
□ Same as above after entering loading.
X Direct switching impossible.
▨ Different in mode switching between VCR body and Remote Control unit.

**NOTES:** 1. The playback mode can be set by the Remote Control unit.
2. The playback mode is set in place of the still state by the Remote Control unit.

**Table 2-6 Possible Mode Switching by V-8000 Remote Control**

| Preset Mode / Switching Mode | STOP | PLAY | PAUSE | RE-VIEW | CUE | Double Speed |
|---|---|---|---|---|---|---|
| Only cassette holder | X | X | X | X | X | X |
| In Loading | Δ | Δ | X | Δ | Δ | Δ |
| EJECT | □ | □ | X | □ | □ | □ |
| REW | O | O | X | O | O | O |
| STOP | | O | X | O | O | O |
| FF | O | O | X | O | O | O |
| PLAY | O | | O Still | O | O | O |
| STILL | O | O Pause Reset | O Pause Reset | O | O | O |
| REC | O | (Note 1) X | O Rec Pause | X | X | X |
| REC Pause | O | X | O Pause Reset | X | X | X |
| AUDIO DUB | O | O | O Audio Dub Pause | O | O | O |
| AUDIO DUB Pause | O | O Play | O Pause Reset | O | O | O |
| REVIEW | O | (Note 2) O | X | | O | O |
| CUE | O | O | X | O | | O |
| Double Speed | O | O | O Still | O | O | |

O Direct switching possible.
Δ Switching after end of loading.
□ Same as above after entering loading.
X Direct switching impossible.
▨ Different in mode switching between Remote Control unit and VCR body.

**NOTES:** 1. The playback mode cannot be set on the VCR body.
2. The still state is set on the VCR body.

**Table 2-7 Mode Switching Priority in Multipressing V-8000 Keys**

| Preset Mode | STOP | EJECT | REW | FF | PLAY | PAUSE | REC | AUDIO DUB | REVIEW | CUE | Double Speed |
|---|---|---|---|---|---|---|---|---|---|---|---|
| STOP | | STOP | ← | ← | ← | ← | ← | ← | ← | ← | ← |
| EJECT | STOP | | EJECT | ← | ← | ← | ← | ← | ← | ← | ← |
| REW | STOP | EJECT | | REW | ← | ← | ← | ← | ← | ← | ← |
| FF | STOP | EJECT | REW | | FF | ← | ← | ← | REVIEW | FF | ← |
| PLAY | STOP | EJECT | REW | FF | | STILL | PLAY | ← | REVIEW | PLAY | ← |
| PAUSE | STOP | EJECT | REW | FF | STILL | | REC PAUSE | AUDIO DUB PAUSE | REVIEW | CUE | Double Speed |
| REC | STOP | EJECT | REW | FF | PLAY | REC PAUSE | | REC | REVIEW | CUE | Double Speed |
| AUDIO DUB | STOP | EJECT | REW | FF | PLAY | AUDIO DUB PAUSE | REC | | REVIEW | CUE | Double Speed |
| REVIEW | STOP | EJECT | REW | REVIEW | ← | ← | ← | ← | | ← | ← |
| CUE | STOP | EJECT | REW | FF | PLAY | CUE | ← | ← | REVIEW | | CUE |
| Double Speed | STOP | EJECT | REW | FF | PLAY | Double Speed | ← | ← | REVIEW | CUE | |

## 2-2-7 Plunger Solenoid Operations

### 1. Energization

The electronic logic circuits in the V-8000T replace the mechanical logic devices in the previous models. For mechanical mode setting, therefore, the present Logic Control Circuit uses a variety of plunger solenoids. Table 2-8 shows the plunger solenoids which are energized in accordance with each mode of operation.

**Table 2-8 Plunger Solenoid Energization for Respective Modes of Operation**

| Solenoid / Mode | EJECT | REW | FF | PLAY | REC | AUDIO DUB | C (CUE) | R (REVIEW) | PAUSE | Double Speed | STILL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EJECT SOLENOID | ○ | | | | | | | | | | |
| REW SOLENOID | | ○ | | | | | | ○ | | | |
| FF SOLENOID | | | ○ | | | | ○ | | | | |
| PLAY SOLENOID Note 1 | | | | ○ | ○ | ○ | | | ○ | ○ | ○ |
| Q/R SOLENOID Note 2 | | | | | | | ○ | ○ | | | |
| PINCH LOCK SOLENOID | | | | ○ | ○ | ○ | | | | ○ | ○ |
| PAUSE Note 3 SOLENOID | | | | | | | | | ○ | | |

Marks ○ indicate energization.

**NOTES:**
1. The play solenoid is energized for approximately 0.5 sec to slacken tape to prevent sticking when the end of loading, fast forward, rewinding, CUE, or review is switched over to the stop state.
2. The cue/review solenoid is not energized for the fast cue or review, (super scanning) when holding the CUE or REVIEW button depressed.
3. The pause solenoid is energized for approximately 0.5 sec when the stop state is switched over to the recording or audio dubbing mode.

## 2. Plunger Solenoid Drive Circuits

The Logic Control Circuit uses two types of plunger solenoids: 2-end, 1-tapped solenoids including the eject, rewinding, fast-forward, play, cue/review, and pinch lock solenoids, and 2-end solenoid including the pause solenoid.

(1) Driving the 2-End, 1-Tapped Solenoid

Each of the 2-end, 1-tapped solenoids is energized in the way that the start tap is decreased for a moment to the low level to lower the impedance for allowing high current enough to attract the plunger. The start tap, then, is recovered to the original level to raise up the impedance, remaining a small current necessary to hold the plunger attracted.

The rewinding solenoid is taken for explanation as the typical solenoid (see Fig. 2-61). If the VCR is set into either of the rewinding or review mode, pin 7 on IC601 changes from the high level to low. This turns Q634 on, the collector of which steps up to 5 V. It is applied to C618 and pin 2 on IC604. The 5 V step-up voltage is differentiated through C618, RL71, and RL75. The differentiated pulse turns the Darlington amplifier, consisting of Q621 and Q627, on for a moment, approximately 50 msec.

The amplifier, then, decrease the start tap of the rewinding solenoid down to around 1 V for the moment. The impedance between the solenoid 12 V end and start tap is as low as the order of ohms. This allows a momentary current as high as approximately 1.6 A to flow the solenoid, which attracts the plunger.

On the other hand, the 5 V step-up voltage applied to pin 2 on IC604 makes the voltage at pin 15 decrease from 12 V to 1 V, which is connected to the hold end of the solenoid. The 1 V voltage allows the hold current to remain flowing through the solenoid even when the start tap rises from 1 V to 12 V. The solenoid, that is, holds the plunger extracted. Note that as the impedance between the solenoid 12 V and hold ends is around 60 Ω, the hold current is 180 to 200 mA.

Of the six 2-end, 1-tapped solenoids, the eject and play solenoids need a particularly high attractive force. The circuit is made to have start current duration as long as 100 msec. This is accomplished in the way that the differential time constant is made longer.

**NOTE:** D614 absorbs negative-going spicks due to differentiation. D621 and D630, also, absorb spikes due to the inductive load.

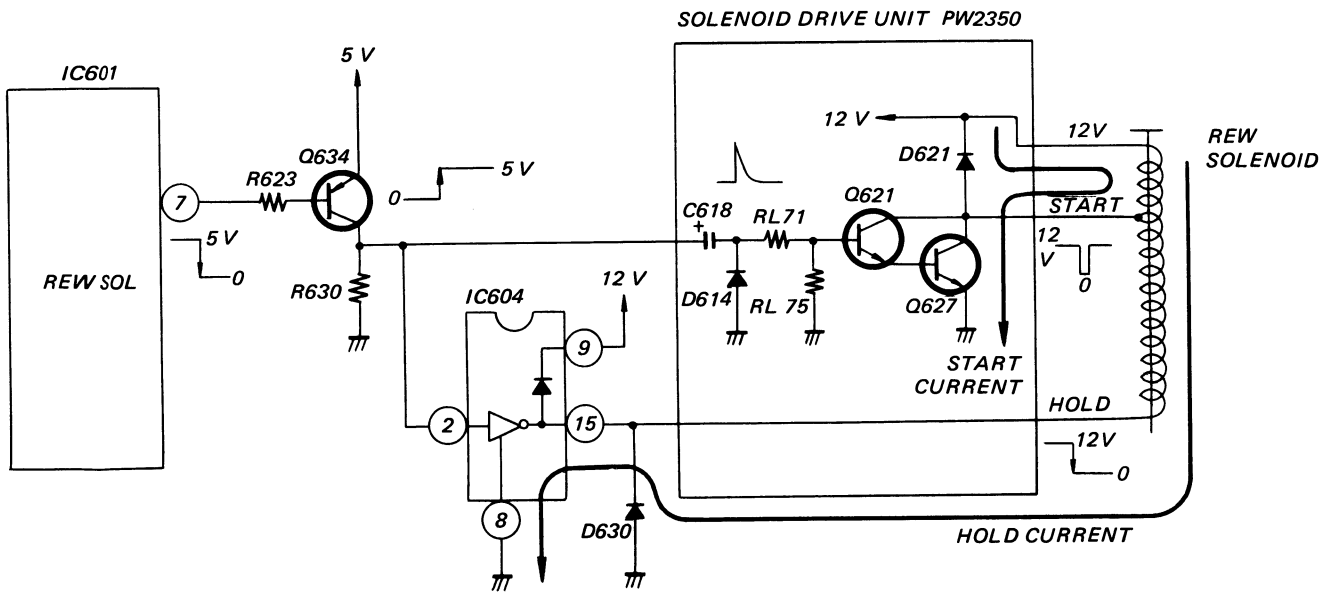



**Fig. 2-61 Rewinding Solenoid Drive Circuit**

**3. Driving the Pause Solenoid (2-end Solenoid)**

If the VCR is set into the pause state, the set signal is delayed a little by the timing adjustment feature (which is explained later) in IC602. It, then, lowers from 5 V to 0 V at pin 13 on. IC602. This turns Q636 on, which produces a 0 V-to-5 V step-up voltage at the collector. The step-up voltage is differentiated through C622, RL80, RL82. The differentiated pulse turns Q640 on for approximately 0.5 sec. The collector voltage of Q640 becomes to 1 V. It allows start current of approximately 1 A to flow through the pause solenoid as the impedance of the pause solenoid is around 10 Ω. The pause solenoid attracts the plunger. After the plunger has been fully attracted, the 5 V voltage at pin 6 on IC604 sets the voltage at pin 11 to 1 V. This allows the pause solenoid to have hold current of approximately 180 mA as 11 V is applied across the impdance of around 10 Ω itself plus the serial 47 Ω resistor.

## 2-2-8 Mode Setting Operation

**1. Loading and Unloading Operations**

**(1) Loading**

If the cassette detect switch is turned on, the voltage at pin 19 on IC601 goes to 0 V and that at pin 20 to 5 V. The former turns Q650 off, which sets the base voltage of Q647 and Q648 to 11.7 V. The latter turns Q619 off, which also turns Q651 off. This sets the base voltage of Q649 to 12 V. Q649, then, is turned off. The eject switch has the contacts 1 and 2 closed during loading. This allows the loading motor to have a voltage of approximately 11.0 V applied. Consequently, the loading current flows in the route of the +12 V line, the collector of Q647, the emitter of Q647, the loading motor, and the ground (see Fig. 2-63).

**(2) Unloading (With EJECT Button Depressed)**

If the EJECT button on the front Control Circuit board is depressed, this prompts the eject solenoid to be energized. The eject solenoid actuates the eject switch to close the contacts 1 and 3. The EJECT button, also, makes pins 19 and 20 on IC601 set to 2 V and 0 V, respectively. The 2 V voltage turns Q650 on, which sets the base of Q647 to 0 V and the base of Q648 to 0.5 V. Q647, then, is turned off and Q648 on. The 0 V voltage, on the other hand, turns Q619 on, which turns Q651 on. This, also, turns Q649 on, the collector of which goes to 11.9 V. Consequently, the loading motor has a voltage of approximately 10.7 V applied in the direction opposite to that of loading. The unloading current flows in the route of the +12 V line, the emitter of Q649, the collector of Q649, the loading motor, the emitter of Q648, the collector of Q648, and the ground. The unloading operation ends when the cassette detect switch is turned off (see Fig. 2-63). Table 2-9 shows major circuit voltages in loading and unloading operations.

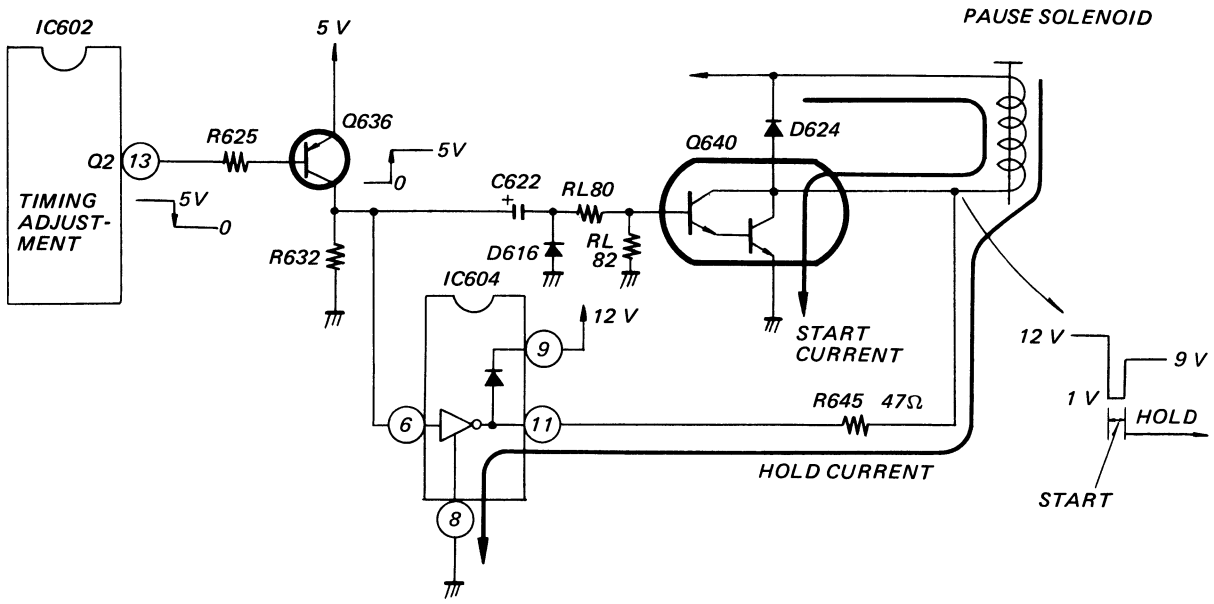
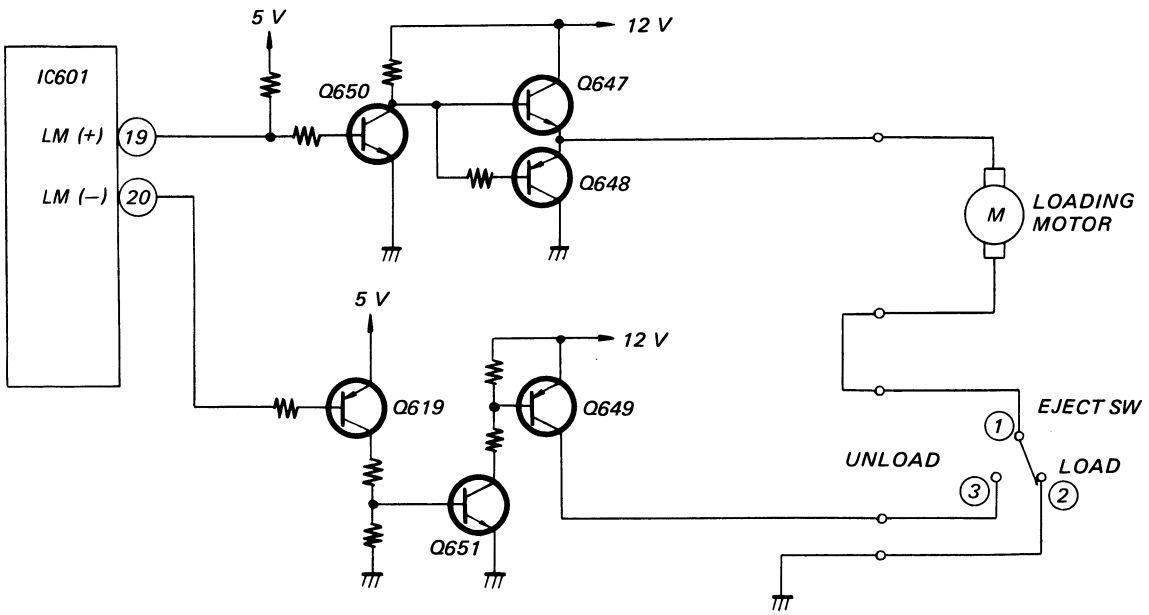



**Fig. 2-62 Pause Solenoid Drive Circuit**

**Table 2-9 Major Circuit Voltage in Loading and Unloading Operations (in V)**

| | IC 601 | | Q647 | | Q648 | Q651 | Q649 | | EJECT SW | Loading Motor |
|---|---|---|---|---|---|---|---|---|---|---|
| | ⑲ | ⑳ | Base | Emitter | Base | Base | Base | Collector | | |
| LOADING | 0 | 5 | 11.7 | 11.0 | 11.7 | 0 | 12 | 0 | 1 and 2 OFF | +11.0 |
| UNLOADING | 2 | 0 | 0 | 1.2 | 0.5 | 0.7 | 11.3 | 11.9 | 1 and 3 ON | −10.7 |




**NOTE:** EJECT SW, which starts after eject solenoid energization as interlocked with eject solenoid.

**Fig. 2-63 Loading Motor Drive Circuit**

In addition, depressing the EJECT button prompts IC601 to feed from pins 26 through 29 the binary signals A through D encoded in accordance with Table 2-10. The encoded binary signals corresponding to the eject action are all at the low level (L). The binary code is decoded through ICL01, pin 1 of which goes to low. The low level makes the EJECT LED light DL01 illuminate. The low level, also, is connected via pin 6 on P601 to the base of Q638 to turn on. The collector of Q638, then, goes to 5 V. The 5 V voltage is connected via pin 3 on P612 to the start tap of the eject solenoid on the solenoid drive unit. A high current flows through the eject solenoid for a moment to extract the plunger. The 5 V voltage, also, is connected to pin 5 on IC604. Pin 12 on IC604 goes to approximately 1 V, which keeps the hold current flowing through the eject solenoid.

**2. Stopping**

When the VCR is reset to the stop state, the encoded binary signals A through D output of pins 26 through 29 on IC601 become all high (H). The decoder IC601 provides no active operation. The solenoid and motor and associated circuits all do not operate; all the mechanisms are in the stop state. Any of the mode settings described in the following sections is generally switched over from the stop state.

**Table 2-10 Operation Code**

| | | D | C | B | A |
|---|---|---|---|---|---|
| IC601 | ENCODE OUT PIN NO. | ㉙ | ㉘ | ㉗ | ㉖ |
| ICL01 | DECODE IN PIN NO. | ⑫ | ⑬ | ⑭ | ⑮ |
| Mode | EJECT | L | L | L | L |
| | REW | L | L | L | H |
| | FF | L | L | H | L |
| | STILL | L | L | H | H |
| | – | L | H | L | L |
| | REC | L | H | L | H |
| | AUDIO DUB | L | H | H | L |
| | CUE (C) | L | H | H | H |
| | REVIEW (R) | H | L | L | L |
| | Double speed (REMOCON) | H | L | L | H |
| | – | H | L | H | L |
| | – | H | L | H | H |
| | – | H | H | L | L |
| | – | H | H | L | H |
| | – | H | H | H | L |
| | STOP or PLAY | H | H | H | H |

### 3. Rewinding Mode Setting

When the REW button is depressed, IC601 outputs the code of binary signals corresponding to the rewinding mode (see Table 2-10) unless the rewinding tape sensor detects the beginning of tape. The encoded signal makes the level at pin 2 on ICL01 go low (L), which illuminates the REW LED light DL02. The low signal, also, is inverted through QL24. The inverted signal is fed as the fast-forward/rewind signal to the Servo Control Circuit.

Also, the encoded signal makes the level at pin 17 (DISK MOTOR) on IC601 go low (L). The low signal is used as the disk motor enable signal with the Servo Control Circuit.

Further, the encoded signal makes the level at pin 7 (REW SOL) on IC601 go low (L), which turns Q634 on. The collector voltage of Q634 goes to 5 V, which enables the rewinding solenoid to attract the plunger (see Fig. 2-61).

### 4. Fast-Forward Mode Setting

When the FF button is depressed, IC601 outputs the code of binary signals corresponding to the fast-forward mode (see Table 2-10) unless the fast-forward tape sensor detects the end of tape. The encoded signal makes the level at pin 3 on ICL01 go low (L), which illuminates the FF LED light DL04. The low signal, also, is inverted through QL24. The inverted signal is fed as the fast-forward/rewind signal to the Servo Control Circuit.

Also, the encoded signal makes the level at pin 17 (DISK MOTOR) on IC601 go low. The low signal is used as the disk motor enable signal with the Servo Control Circuit.

Further, the encoded signal makes the level at pin 8 (FF SOL) on IC601 go low, which turns Q635 on. The collector voltage of Q635 goes to 5 V, which allows a high current to flow for a moment form the +12 V line through the fast-forward solenoid to the start tap, Q622, Q628, and the ground.

On the other hand, the hold current flows from the +12 V line through the fast-forward solenoid to the hold end, pin 14 on IC604, and the ground. The fast-forward solenoid, then, is energized to attract and hold the plunger. For the method of driving the fast-forward solenoid, refer to Section 2-2-7-2-(1).

### 5. Recording Mode and Recording Pause State Setting

#### (1) Recording Mode Setting

When the REC button is depressed, the level at pin 17 on IC601 goes low (L) if the recording INH switch is off. The low signal allows the disk motor enable signal to be fed to the Servo Control Circuit. The level at pin 6 on IC601, in turn, goes low, which turns Q633 on. The collector voltage of Q633 goes to 5 V, which enables the play solenoid to attract and hold the plunger. The level at pin 9 on IC601, in turn, goes low, which makes the level at pin 5 on IC602 go low. This allows the level at pin 1 on IC602 to go low when the leading edge of the PG pulse comes as the clock to pin 3 on IC602. The low signal turns Q637 on. The collector voltage of Q637 goes to 5 V, which enables the pinch lock solenoid to attract and hold the plunger. This makes the pinch roller to be pressed to the capstan to feed tape.

In the recording mode setting, the base voltage of Q633 is raised up to 5 V. Otherwise, when Q658 is turned on in the rewinding mode with the rewinding sensor detecting the beginning of tape and with the play solenoid not energized for the high level at pin 6 on IC601, current flows into the base of Q658. This sets pin 6 on IC601 to unstable high level, which may turn Q633 on. Q633, then, misenergized the play solenoid.

Depressing the REC button prompts IC601 to output from pins 26 through 29 the code of binary signals corresponding to the recording mode (see Table 2-10). The encoded signal makes the level at pin 6 on ICL01 go low (L). The low signal makes the switch eliminating light DL03 and mode indicator light DL07 turn on. The low signal is connected from pin 1 on PL10 through pin on P601 to pin 8 on IC603.

Since pin 17 on IC601 is at the low level in recording, the level at pin 9 on IC603 goes low and the NOR gate output pin 10 on IC603 goes high. This turns Q643 on, which alos turns Q652 on. The collector voltage of Q652 goes to 12 V. The 12 V voltage is fed through P615 and P616 to the Audio Circuit and Video Circuit as the recording +B voltage.

#### (2) Recording Pause State Setting

When the PAUSE button is depressed during recording, the level at pin 13 (PAUSE LED) on IC601 goes low (L). This makes the PAUSE state indicator LED light DL05. The level at pin 9 (PINCH LOCK SOL) on IC601, in turn, changes from the low (L) level to high (H) and the one at pin 10 (PAUSE SOL) on IC601 changes from the high (H) level to low. These signals are synchronized with the PG pulse for timing adjustment by IC601. The level at pin 1 on IC602, then, changes from the low level to high and the one at pin 13 changes from the high level to low. Q637, also, changes from the "on" state to "off" and Q636 changes from the "off" state to "on". These release the pinch lock plunger and make the pause plunger be attracted and held in. Note that the pin 17 (DISK MOTOR) on IC601 remains at the low level. The disk motor keeps revolving.

### 6. Audio Dubbing Mode and Audio Dubbing Pause State Setting

#### (1) Audio Dubbing Mode Setting

When the AUDIO DUB button is depressed the level at pin 17 on IC601 goes low (L) if the recording INH switch is off. This allows the disk motor enable signal to be fed to the Servo Control Circuit. The level at pin 6 on IC601, in turn, goes low, which turns Q633 on. The collector of Q633 goes to 5 V. This enables the play solenoid to attract and hold in the plunger. The level at pin 9 on IC601, then, goes low and the one at pin 5 on IC602 goes low. This allows the level at pin 1 on IC602 to go low when the leading edge of the PG pulse comes as the clock to pin 3 on IC602. The low signal turns Q637 on. The collector voltage of Q637 goes to 5 V, which enables the pinch lock solenoid to attract and hold the plunger.

Depressing the AUDIO DUB button prompts IC601 to output from pins 26 through 29 the code of binary signals corresponding to the audio dubbing mode (see Table 2-10). The encoded signal makes the level at pin 7 on ICL01 go low. The low signal makes the light DL06 illuminate. The low signal, also, is connected from pin 2 on PL10 through pin 2 on P601 to pin 6 on IC603.

Since pin 17 (DISK MOTOR ON) on IC601 is at the low level in audio dubbing, the level at pin 5 on IC603 goes low and the NOR gate output pin 4 on IC603 goes high. This turns Q644 on, which also turns Q653 on. The collector voltage of Q653 goes to 12 V. The 12 V voltage is fed through pin 2 on P615 to the Audio Circuit as the audio dubbing +B voltage.

Since Q644 is on, its collector is at the low level. This decreases the base potential of Q654 through D635 to turn on. The collector voltage of Q654 goes to 12 V. The 12 V voltage is fed as the playback and audio dubbing +12 V voltage to the Servo Control Circuit and to the Video Circuit through pin 2 on P505.

#### (2) Audio Dubbing Pause State Setting

LED light illumination, solenoid energization, and disk motor revolving operations in the audio dubbing pause state setting, are similar to the ones in the recording pause state setting described in Section 2-2-8-5-(2).

In the audio dubbing pause state setting, pin 13 on IC601 is at the low (L) level. This turns Q660 on. Pin 2 on P601 is also at the low level. This turns Q659 on. The collector level of Q659, then, is high. The high signal is fed to the Servo Control Circuit as the audio muting release signal.

## 2-2-9 Playback Mode and Still State Setting

### 1. Playback Mode Setting

The playback mode setting operations is the same as the recording mode setting operation that the play solenoid and pinch lock solenoid are energized. When the PLAY button is depressed, the level at pin 12 on IC601 goes low (L). This illuminates the light DL09 through R609. Note that in the playback mode setting operation, IC601 does not output any active code of binary signals from pins 26 through 29, but the decoder ICL01 operates in the same way as in the stop state setting operation. The levels at pins 12 and 17 on IC601, also, go low. These make the levels at pins 1 and 2 on IC603 go low. These make the NOR gate output pin 3 go to the high (H) level. This high level turns Q645 on, which turns Q639 on. The collector voltage of Q639 becomes 12 V. The 12 V voltage is connected through pin 3 on P615 to the Audio Circuit as the playback signal. Since Q645 is on, its collector level is low. This decreases the base potential of Q654 through D634. The decreased base potential turns Q654 on. The collector voltage of Q654 goes to 12 V. The 12 V voltage is fed to the Servo Control Circuit as the playback and audio dubbing +12 V voltage and through pin 2 on P505 to the Video Circuit.

### 2. Still State Setting

If the PAUSE/STILL button is depressed during playback, the VCR is set into the still state. The level at pin 13 on IC601, then, goes to the low level. The low level illuminates the STILL LED light DL05. Pins 26 through 29 on IC601 output the code of binary signals corresponding to the still state (see Table 2-10). The encoded signal makes the level at pin 4 on ICL01 go low (L). The low level turns QL25 on: The collector voltage of QL25 becomes high (H). The high signal is fed through pin 4 on PL10 and pin 4 on P601 to the Servo Control Circuit as the still state signal.

The still state setting operation is different from the recording pause state setting operation and the audio dubbing pause state setting operation in that the tape running by the capstan motor is stopped with leaving the pinch lock solenoid energized. The operation of the pause solenoid is the same as in the recording pause state setting operation or in the audio dubbing pause state setting operation.

### 2-2-10 Cue Mode Setting

When the CUE button is depressed, IC601 outputs from pins 26 through the code of binary signals corresponding to the cue mode (see Table 2-10). The encoded signal makes the level at pin 9 on ICL01 go low (L). The low level illuminates the CUE LED light DL10. The level at pin 8 on IC601, on the other hand, goes low. The low level turns Q635 on. This enables the fast-forward solenoid to attract and hold the plunger. The low level at pin 7 on ICL01 is connected through DL52 and pin 3 on PL10 and pin 3 on P601 to D607 and the base of Q632 as the cue and review signal (active low signal). The active low signal makes the level at pin 1 on IC603 go low. This turns Q632 on. Since the level at pin 17 on IC601 is low in the cue mode of operation, the level at pin 2 on IC603 also goes low. The level at pin 3 on IC603 becomes high. The following operation is similar to that of the playback mode setting operation. As a result, the play +12 V voltage is fed to the Audio Circuit and the playback and audio dubbing +12 V voltage to the Servo Control Circuit and Video Circuit.

On the other hand, since Q632 is on, its collector level is high. The low level at pin 17 on IC601 turns Q655 on. This makes the collector level of Q655 also go high. This allows C633 to keep charging current unless QL27 is turned on by **holding** the CUE button SL10 or REVIEW button SL08 depressed. The charging current turns Q656 off, which turns Q657 on. This enables the cue and review solenoid to attract and hold the plunger (see Fig. 2-64).

The disk motor enable signal is fed to the Servo Control Circuit with the level at pin 17 on IC601 being low. The cue and review signal, also, is fed to the Servo Control Circuit with the collector level of Q632 being high.

### 2-2-11 Review Mode Setting

When the REVIEW button is depressed, IC601 outputs from pins 26 through 29 the code of binary signals corresponding to the review mode (see Table 2-10). The encoded signal makes the level at pin 10 on ICL01 go low. The low signal illuminates the REVIEW LED light DL08. The level at pin 7 on IC601, on the other hand, goes low, which turns Q634 on. This enables the rewind solenoid to attract and hold the plunger. The low level at pin 10 on ICL01 passes DL51 and then is input to the OR circuit together with the review signal from DL52. The output of the OR circuit is applied to Q632. The following operation is similar to that of the cue mode setting operation described in Section 2-2-10 (see Fig. 2-64).

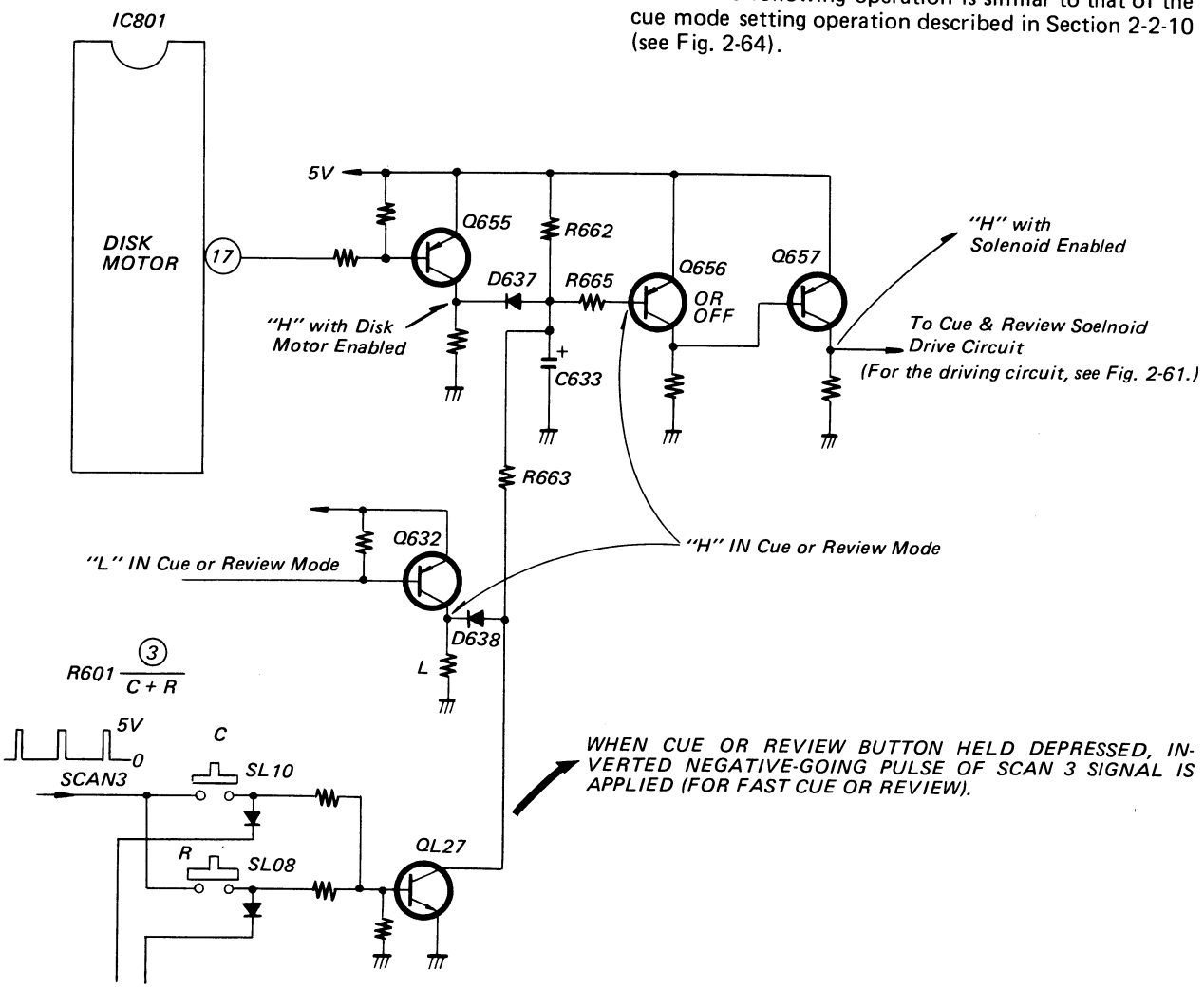



**Fig. 2-64 Cue and Review Solenoid Drive Signal Circuit**

### 2-2-12 Fast Cue and Review (Super Scan) Mode Setting

In the fast cue or review mode of operation, the picture can be played back as high as three times the normal cue or review playback, or as high as 30 times the ordinary playback, with holding the CUE or REVIEW button depressed. Setting the VCR in the fast cue or review mode deenergizes the cue and review solenoid which has attracted and held in the plunger. Fig. 2-64 illustrates the fast cue and review mode setting operation.

In the normal cue or review mode of operation, QL27 is off. The high collector level of Q632 and the high collector level of Q655 are allowed to directly turn Q656 off. C633 is charged. If **holding** the CUE or REVIEW button **depressed,** on the other hand, the scan 3 pulse is applied directly to QL27. Only when the pulse is high, QL 27 is turned on. The collector of QL27 goes to the low level. This discharges C633.

Then, we will consider about the time constants of charging and discharging of C633. In charging, current flows through R662 (20 kΩ) and R665 (20 kΩ) to C633. In discharging, current flows through R663 (200 Ω) from C633. The time constant of charging, thus, takes longer time than that of discharging. Consequently, the positive end of C633 cannot rise up to the high level. The result is that Q656 turns on. This turns Q657 off, which deenergizes the cue and review solenoid.

### 2-2-13 Double Speed Mode Setting (Only for Remote Control)

If the VCR is set in the double speed mode by the Remote Control unit, the code of binary signals corresponding to the double speed mode is output from pins 26 through 29 on IC601 (see Table 2-10). The encoded signal makes the level at pin 11 on ICL01 go low (L). The low signal illuminates the double speed LED light DL14. The low signal, also, is fed as the double speed signal through pin 5 on PL10 and pin 5 on P601 to the Servo Control Circuit. The low signal, further, passes D608 and then makes the level at pin 1 on IC603 go low.

The level at pin 12 on IC601 is high, which reverse-biases D611. The following operation is similar to that of the playback mode setting operation except that the PLAY LED light does not illuminate.

### 2-2-14 Antenna Switching

The antenna selector (TV-VCR selector) has two positions: TV and VCR. In the TV position, the level at pin 16 on IC601 is high; in the VCR position, it is low. In the VCR position, the TV-VCR LED indicator DL11 is lit through R608. The TV and VCR settings are alternated one after another whenever depressing the switch SL11. Note that when power is turned on, the selector is initially at the TV position. When any of the PLAY, AUDIO DUB, CUE, REVIEW, and Double Speed button is depressed, the selector is forcibly set to the VCR position.

In the VCR position, the level at pin 16 on IC601 is low. This turns Q646 off. The collecto voltage of Q646 goes to approximately 11 V. The voltage is connected through pin 3 on P605 to the Antenna Terminal board. The low signal, also, turns Q661 on. This allows the emitter of Q661 to feed the 12 V voltage to the modulator circuit as the power voltage.

### 2-2-15 Fault Detection Operation

#### 1. Tape End Sensor

If the end of tape is detected, pin 4 on IC605 goes to the low (L) level (refer to Section 2-2-4). The low level turns Q615 on. This allows the scan 2 signal to pass Q615 to the input pin 35. The microcomputer determines the signal as the tape end and then prompts the VCR to enter the stop state. If the auto-rewinding switch is on, then the VCR is switched over to the rewinding mode of operation.

#### 2. Tape Beginning Sensor

When the beginning of tape is detected, pin 18 on IC605 goes to the low (L) level (refer to Section 2-2-4). Since the level at pin 6 (PLAY SOL) on IC601 is high (H), however, Q658 is on. The low signal, therefore, turns Q616 on. This allows the scan 2 signal to pass Q616 to the input pin 34. The microcomputer determines the signal as the beginning of tape and then prompts the VCR to enter the stop state.

In the present logic control system, the rewind oscillator is forcibly stopped while the play solenoid is energized. This is done in the way that the low level at pin 6 on IC601 is connected through D609 to pin 21 IC605 to make this go low. The reason of forcibly stopping the rewind oscillator is to prevent possible heat resulting on the TV screen from the tape sensor oscillator with the rewind sensor placed in the physical vicinity ofthe pair of video heads.

As described previously, Q658 controls the output (pin 18 on IC605) of the rewind sensor. When the playback mode of operation is to be switched over to the rewinding mode, for example, the low signal at pin 18 on IC605 is to turn Q616 on directly. This leads to that the rewind oscillator is regarded to be not in operation. This inhibits the playback mode from being switched over to the rewind mode. To prevent such a wrong operation, Q658 arranged so that Q616 this is turned off and cannot be turned on by the low signal at pin 18 on IC605.

#### 3. Dew Sensor

If dew is detected, then pin 6 on IC605 goes to the high (H) level (refer to Section 2-2-4). The level at pin 12 on IC603, then, goes high. The high level holds the level at pin 11 on IC603 low at all times irrespective of the level at pin 13. The low signal is input to pin 5 on IC601 for switching over to the stop state.

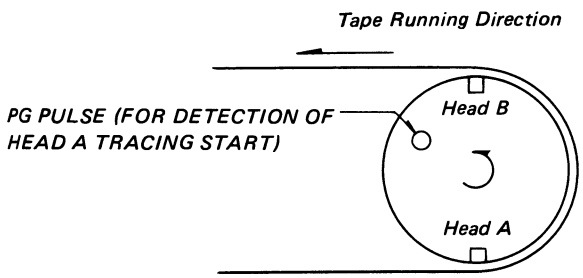
4. **Slack Sensor**
If some tape slack is detected, a 5 V voltage is connected to pin 1 on P608. The voltage makes the level at pin 13 on IC603 to go high (H). The high level holds the level at pin 11 on IC603 low at all times irrespective of the level at pin 12. The low signal is input to pin 5 on IC601 for switching over to the stop state.

5. **Disk Motor Revolution Sensor**
If the disk motor fails to revolve with some cause, pin 10 on IC605 has no switching pulse. Pin 12 on IC605, then, goes to the low level. The low level is connected to pin 3 on IC601 for switching over to the stop state.

## 2-2-16 Timing Adjustment Circuit

1. **General**
The timing adjustment circuit used in the present logic control system is provided for synchronizing the instants of setting and resetting the VCR into the pause state or the instants of energizing and deenergizing the pause solenoid and pinch lock solenoid, with the PG pulse. Such a synchronization assures that the train of control pulses can be recorded in a regular form. The regular train prevents tracing disturbance of the pair of video heads in the vicinity of a spliced portion of tape in an edition recording with use of the pause function, thereby maintaining uniform reproduced picture.

2. **Principles of Operation**
For ease of explanation, assume that the PG pulse be generated when the head A is to start tracing, or the head B is to finish tracing, as illustrated in Fig. 2-65.




*Note: The PG pulse is generated when the head A starts tracing.*

**Fig. 2-65 PG Pulse Generation**

If the pause state set and reset instants are made at the same PAUSE button on-off instants, either head A or B is in the final tracing upon setting for the pause state. Either head A or B, also, is in the first tracing upon resetting from the pause state. The tracing head, further, is at any position on the tape pattern upon setting for or resetting from the pause state. The heads, thus, trace on the tape as illustrated in Fig. 2-66 (1) and (2). It could occur that in playback, the heads A and B cannot regularly alternated one after another in the tracing order. In such an event, noise could appear on the reproduced picture in the vicinity of the pause spliced portion. The new timing adjustment circuit adjusts the pause state set and reset instants to the head A tracing start instant, or the head B tracing finish instant, at any time. This means that the heads A and B can be alternated one after another in the regular tracing order at any time.

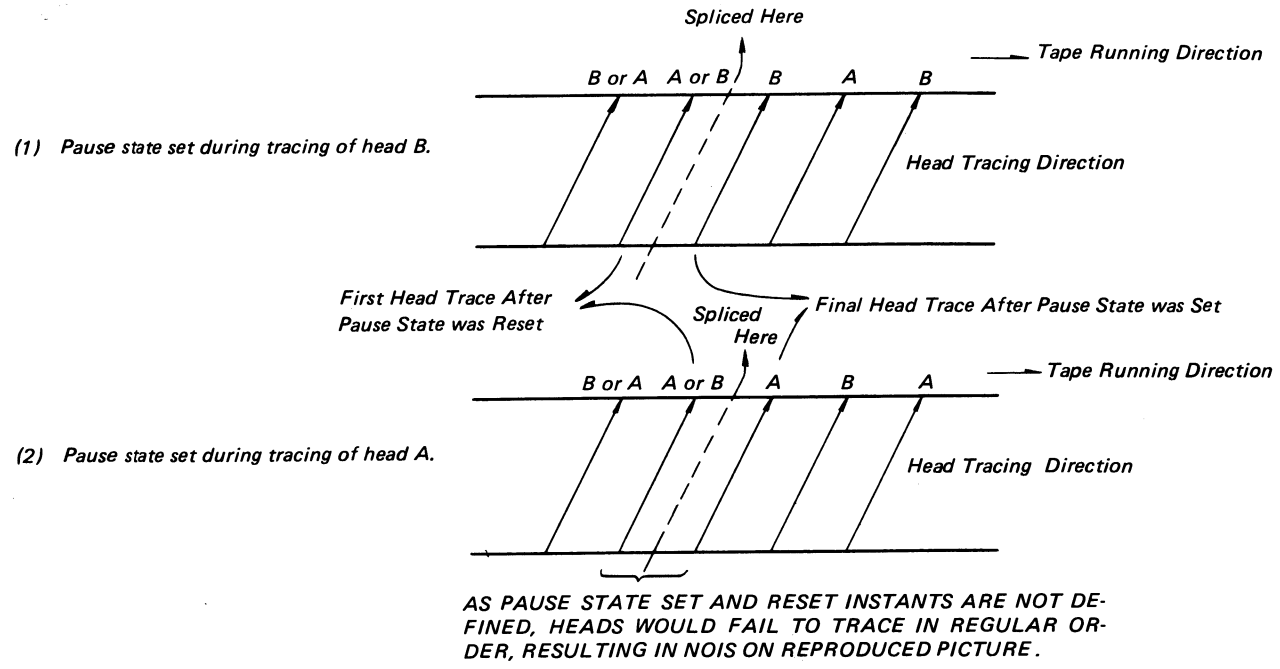



**Fig. 2-66 Illustrative Head Tracing Pattern of Previous Splicing Recording Fashion**

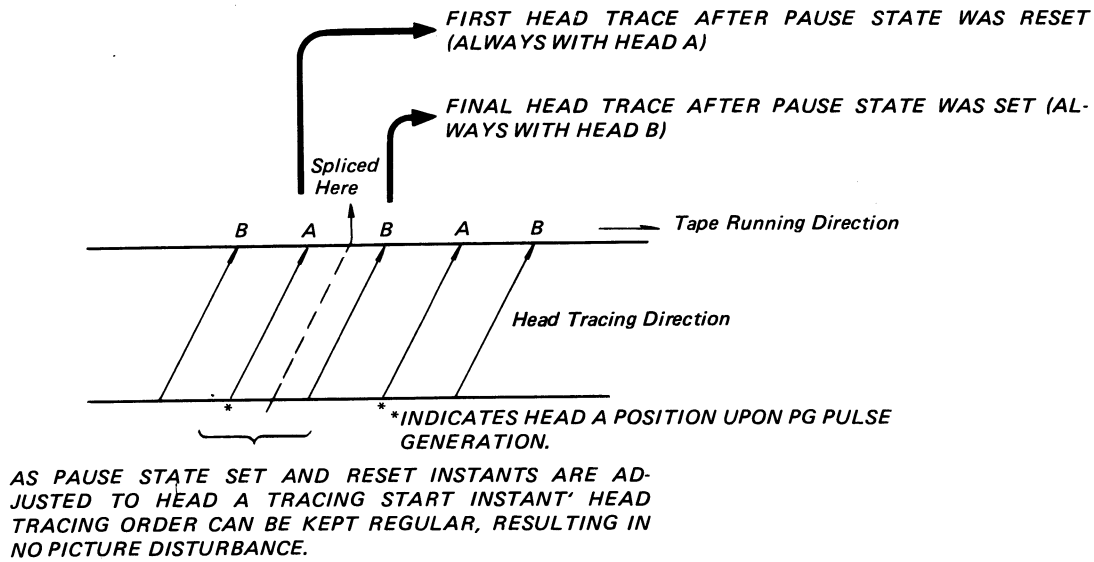



**Fig. 2-67 Illustrative Head Trace Pattern of New Timing Adjustment Circuit.**

**Table 2-11 Advantages of Timing Adjustment Circuit Compared with Previous Arrangement**

| | Previous Arrangement | New Timing Adjustment Circuit |
|---|---|---|
| Final Tracing Head Pause State Set | Either A or B | Always B |
| First Tracing Head Upon Pause State Reset | Either A or B | Always A |
| Head Position Upon Pause State Set or Reset | Not defined | Lower tape edge (marked with * in Fig. 2-67) |

### 3. Circuit Operation

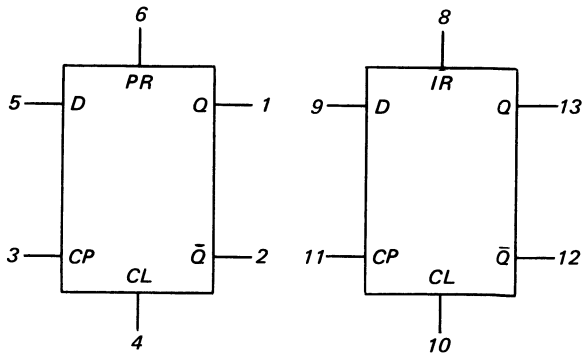
**Upon setting the pause state** for which the pinch lock solenoid is deenergized and the pause solenoid is energized, logical state changes are as follows.
LOW at IC601 pin 9 to HIGH for IC602 pin 5.
HIGH at IC601 pin 10 to LOW for IC602 pin 9.
The leading edge of the PG pulse delivered from the collector of Q642 changes:
LOW at IC602 pin 1 to HIGH, which deenergizes the pinch lock solenoid.
HIGH at IC602 pin 13 to LOW, which energizes the pause solenoid.
**Upon resetting the pause state** for which the pinch lock solenoid is energized and the pause solenoid is deenergized, logical state changes are as follows.
HIGH at IC601 pin 9 to LOW for IC602 pin 5.
LOW at IC601 pin 10 to HIGH for IC602 pin 9.
The leading edge of the PG pulse delivered from the collector of Q642 changes:
HIGH at IC602 pin 1 to LOW, which energizes the pinch lock solenoid.
LOW at IC602 pin 13 to HIGH, which deenergizes the pause solenoid.
The resistor R646 initializes Q1 and Q2 to the high state when power is turned on. In the event the PG pulse will not come in with some cause when the pinch lock solenoid or pause solenoid needs to be deenergized, then the level at pin 9 on IC601 is made high through D633, or the level at pin 10 on IC601 is made high through D636. The high signal makes PR1 or PR2 high, thereby deenergizing the pinch lock solenoid or pause solenoid.

Upon setting the pause state, there is a timing difference of approximately 9 μsec between the instant when the low level at pin 9 on Q601 changes high and the instant when the high and the instant when the high level at pin 10 on IC601 changes low. The timing difference is due to the software programming time because of different ports. The timing difference could cause presetting, which results in deenergization of the pinch lock solenoid before the leading edge of the clock. To avoid such a failure, C624 is provided to absorb the spike. Fig. 2-69 is an operation time chart for the timing adjustment circuit.

**Table 2-12 TC4013BP Truth Table**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| CL | PR | D | CP Δ | $Q_n + 1$ | $Q_n + 1$ |
| L | H | ⁚ | ⁚ | H | L |
| H | L | ⁚ | ⁚ | L | H |
| H | H | ⁚ | ⁚ | L | H |
| L | L | L | ⎍ | L | H |
| L | L | H | ⎍ | H | L |
| L | L | ⁚ | ⎍ | $Q_n$ * | $Q_n$ * |

⁚ : Don't Care
Δ : Level Change
* : No Change




$V_{DD}$: 14, $V_{SS}$: 7

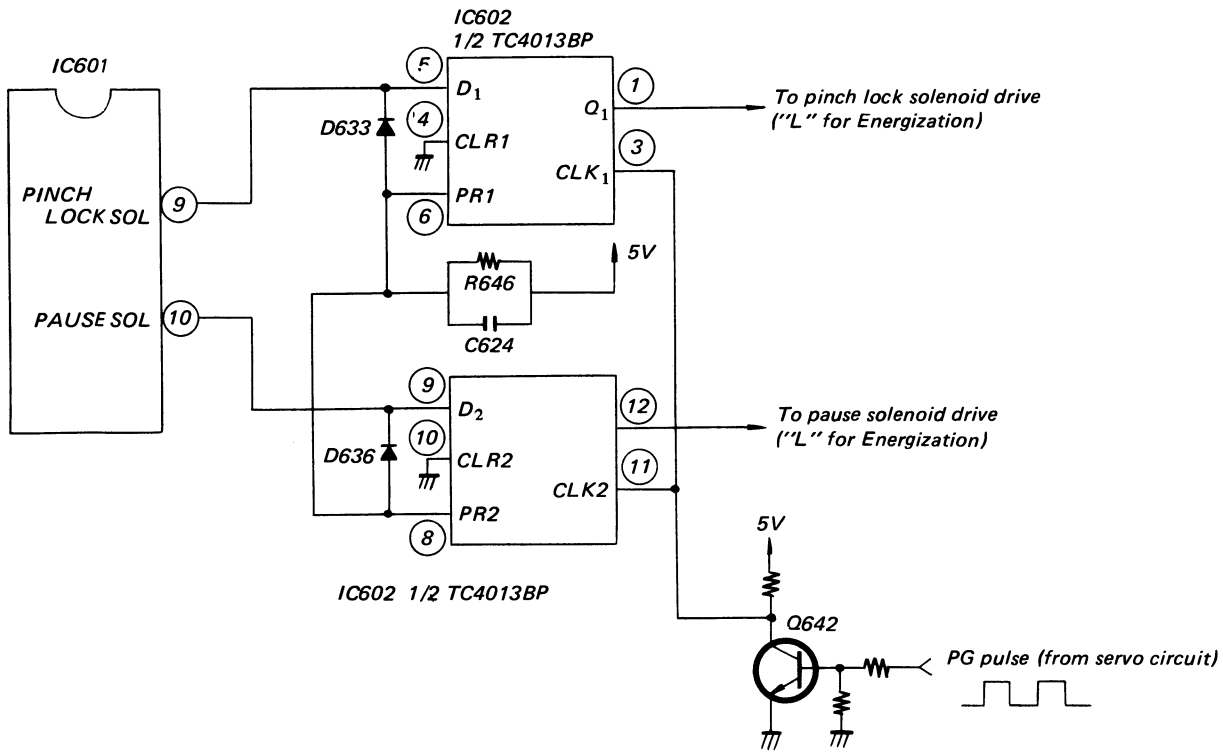



Fig. 2-68 Timing Adjustment Circuit

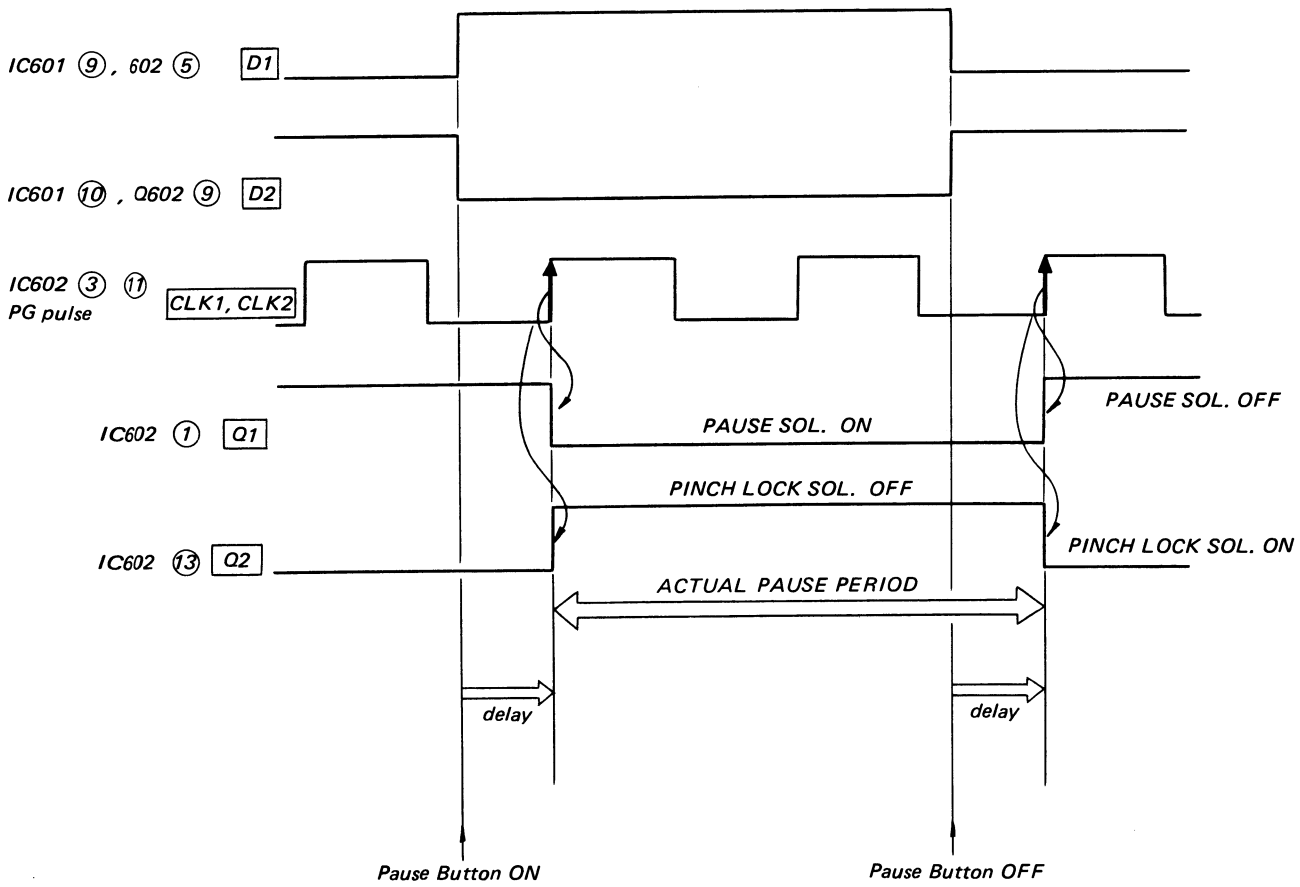



Fig. 2-69 Timing Adjustment Circuit Operation Chart

## 2-3 REMOTE CONTROL SYSTEM

### 1. General

For use of the Remote Control System in the V-8000, the VC-101 of the Control Unit is the wired remote control which is used to control the VCR remotely. The VC-101 is capable of remotely controlling six modes of operation: playback, cue, review, pause, double speed, and stop.

### 2. Circuit Description

A signal fed from the VC-101 is converted by ICR01 to a form acceptable input to the microcomputer ICL01 in the Logic Control unit, ICR01 (TC4532BP) is the 8-bit encoder that receives eight input signals, detects the signal of the highest level from among the eight signals, and outputs the corresponding signal in bits.

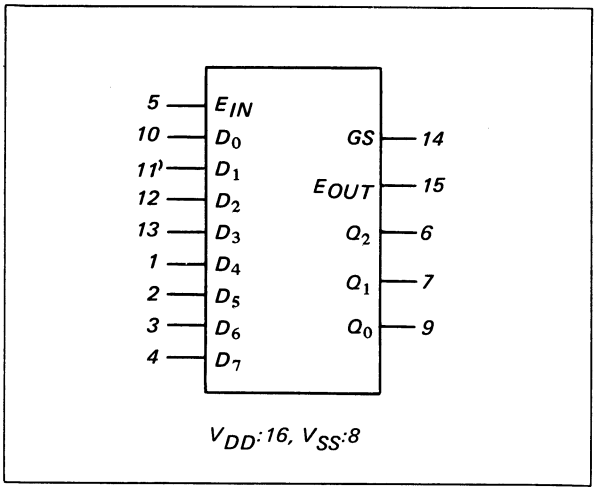



**Fig. 2-70 ICR01 TC4532BP or CD4532BE BLOCK DIAGRAM**

The output signal of ICR01 is inverted through the NOR gate in ICR02. The inverted signal is fed to the Logic Control Circuit (PW2235).

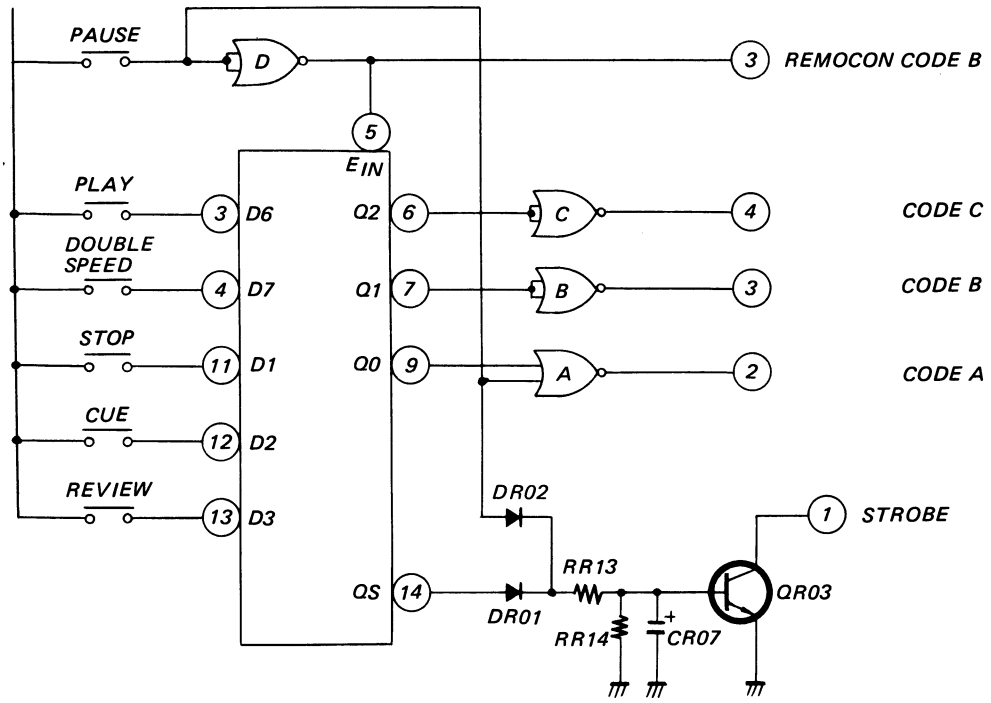
If the PLAY, CUE, REVIEW, DOUBLE SPEED, or STOP button on the VC-101 are depressed, the corresponding signal is input to the ICR01, which feeds out the high-level signal from pin 14 (GS) irrespective of the kind of input signal. The output signal at pin 14 is used for judging whether the input signal is present or absent, ICR01, on the other hand, feeds out binary signals corresponding to the input signals from pin 9 (Q0), pin 7 (Q1), and pin 6 (Q2). Those output binary signals are inverted through the NOR gates A, B, and C, respectively. The inverted signals consist of the remote control signals, which are transmitted to the electronic Logic Circuit.

If the PAUSE button is pressed, the pause operation signal is inverted through the NOR gate D to the low-level (0 V). The inverted low-level signal is applied to pin 5 ($E_{IN}$). This prompts ICR01 to set all outputs to the low level. Instead, the pause operation signal is input to the NOR gates A and D, which form a binary signal for the pause mode of operation.

**Table 2-13 Truth Table**

| INPUT | | | | | | | | | OUTPUT | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $E_{IN}$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | GS | $Q_2$ | $Q_1$ | $Q_0$ | $E_{OUT}$ |
| L | :: | :: | :: | :: | :: | :: | :: | :: | L | L | L | L | L |
| H | L | L | L | L | L | L | L | L | L | L | L | L | H |
| H | H | :: | :: | :: | :: | :: | :: | :: | H | H | H | H | L |
| H | L | H | :: | :: | :: | :: | :: | :: | H | H | H | L | L |
| H | L | L | H | :: | :: | :: | :: | :: | H | H | L | H | L |
| H | L | L | L | H | :: | :: | :: | :: | H | H | L | L | L |
| H | L | L | L | L | H | :: | :: | :: | H | L | H | H | L |
| H | L | L | L | L | L | H | :: | :: | H | L | H | L | L |
| H | L | L | L | L | L | L | H | :: | H | L | L | H | L |
| H | L | L | L | L | L | L | L | H | H | L | L | L | L |

:: Don't Care




| INPUT | REMOCON CODE | | | |
|---|---|---|---|---|
| | A | B | C | D |
| PAUSE | L | H | H | L |
| PLAY | H | L | L | H |
| DOUBLE SPEED | L | L | L | H |
| STOP | L | H | H | H |
| CUE | H | L | H | H |
| REVIEW | L | L | H | H |

**Fig. 2-71 Remocon Circuit**

In the figure, QR03 produces the strobe signal which is delayed by approximately 20 msec after an operation button on the VC-101. VCR Control Unit has been pressed. The strobe signal, then, prompts the microcomputer ICL01 in the electronic Logic Control Circuit to read the input remote control signal, which controls the VCR operation.

## 3-1. AUDIO SYSTEM

### 3-1-1. Input Circuit

The V-8000 VCR can receive an audio signal input either from the Tuner or the AUDIO IN terminal according to the position of the INPUT SELECT switch being in either the TV or LINE position. The standard input signal level is -10 dBs. The microphone has higher priority than any other input audio signals irrespective of the INPUT SELECT switch position if plugged into the MIC jack INPUT on the front panel. The microphone, therefore, must be unplugged if not in use. The standard signal level at the MIC jack is -70 dBs and the input impedance should be 4.7 kΩ.

### 3-1-2. Audio Head Switching Circuit

The audio head switching circuit, consisting of Q702, Q707, Q708, and Q709, switches connection of the audio head with the playback amplifier input or the recording amplifier output in the way described below.

In the E-E or playback mode of operation, Q709 is turned on. This drives Q707 and Q708, which are turned on. These ground the recording signal and at the same time, also, ground one of the audio head leads. The transistor Q702, which is turned off upon playback and muting resetting only, feeds the playback signal into Q703. Upon E-E and recording (including audio dubbing), Q702 is turned on to ground the input of the playback amplifier and at the same time, grounds one of the audio head leads through a minute resistor.

In the recording (including audio dubbing) mode of operation, Q709 is turned off, which turns Q707 and Q708 off. These allow the recording signal to be applied to the audio head.

### 3-1-3. Amplifiers and AGC Circuit

The Audio Circuit has four amplifiers and an AGC (automatic gain control) circuit, which consist of IC701: (1) one is a microphone pre-amplifier having a signal input at pin-16, a signal output at pin-14, a negative feedback input at pin-15, and a gain of approximately 30 dB, (2) another is a drive amplifier having a signal input at pin-3, a signal output at pin-5, and a gain of approximately 30 dB, (3) still another is an output amplifier having a signal input at pin-6, a signal output at pin-10, and a gain of approximately 20 dB, and (4) the last is a recording amplifier having a signal input at pin-7, a signal output at pin-9, and a gain of approximately 20 dB. The AGC circuit has a variable resistor connected between pin-2 and ground and a control signal input at pin-1.

### 3-1-4. Playback Equalizer Circuit

The playback equalizer circuit consists of Q703, Q704, Q705, C702, R705, R715, C708, R716, R751, C709, and R717. The transistor-FET direct-coupled amplifier, consisting of Q703 and Q704, magnifies the small playback signal output of the audio head with a sufficient gain and high signal-to-noise ratio. The ripple filter, consisting of Q705, prevents the power signal-to-noise ratio.

The negative feedback circuit, consisting of R715, R716, R751, and C708, in the playback amplifier, consisting of Q703 and Q704, changes the impedance with the frequency. With the impedance change, the playback amplifier provides a dropping frequency response from midrange to bass frequencies and a flat frequency response at treble frequencies.

In the LP (long play), or βIII format, mode of operation, the series circuit, consisting of C709 and R717, is grounded to decrease the amount of negative feedback at the midrange to treble frequencies.

### 3-1-5. ALC Circuit

The ALC (automatic level control) circuit, consisting of IC701, D702, D704, and D705, automatically controls the amplifier gain or attenuates the recorded signal. More details are explained as follows.

In the E-E or recording mode of operation, the output audio signal is rectified through D704 and D705 to convert the volume change of sound to level variation of DC voltage. The DC voltage which is connected to pin-1 on IC701 changes the impedance between pin-2 and ground. The circuit of changing impedance and R748 or R736 in use of the microphone forms an attenuator which automatically controls the amplifier gain. The impedance decreases with a positive-going increase of the level of DC voltage. The result is a high output audio signal level attenuation.

In the playback mode of operation, the playback +B voltage is connected through R769 and D702 to pin-1 on IC701. This attenuates the recorded signal to prevent this from leaking out.

### 3-1-6. Microphone Amplifier

The microphone amplifier, consisting of Q710, has a gain of approximately 15 dB. The two amplifier stages made up of this amplifier and the previously-mentioned microphone pre-amplifier having a signal input at pin-16 and a signal output at pin-14 in IC701, serves to prevent the microphone input signal from leaking out in the playback mode of operation.

### 3-1-7. Recording Compesating Circuit

The recording compensating circuit, consisting of R792, C732, and C733, operates as follows. The pin-9 on IC701 supplies the recording audio signal having a flat frequency response. The audio signal is made to flow as the recording current through the current regulating resistor R792 into the audio record/playback head in recording mode. The recording current is increased at treble frequencies in a slope determined in terms of the time constant of R792 and C733 placed in parallel with each other. The recording current, further, is raised up particularly around a peaking point at which the audio record/playback head and C733 resonate. In the LP (long play), or βIII format, mode of operation, C732 is connected in parallel with C733 to lower the resonant frequency of the audio record/playback head to further compensate the recording current at the treble frequencies.

### 3-1-8. Switching Circuits

The Audio Circuit has five switching circuits, consisting of Q711 through Q715, which are described in detail below. The switching circuit of Q711 is turned on when a signal is input either from the Tuner or AUDIO IN terminal to ground the microphone input signal from the MIC jack. If the microphone is plugged in Q711 is turned on by the playback +B voltage which grounds the microphone input signal when in the playback mode of operation.

The switching circuit of Q712 is turned on at the same time when the microphone is plugged into the MIC jack input. This turns Q711 off, which connects the microphone input signal to pin-3 on IC701.

The switching circuit of Q713, to the base of which the playback +B voltage and microphone +B voltage are connected to through resistor R746, grounds the audio signal input either from the Tuner or AUDIO IN terminal in the playback mode of operation when the microphone is plugged in.

The switching circuit of Q714 is turned off only in the playback and muting resetting modes of operation to connect the playback audio signal to pin-3 on IC701.

The switching circuit of Q715 is turned on in the playback mode of operation if the playback +B voltage is connected to the base through resistor R766. It quickly discharges C716 to prevent this from activating the ALC circuit.

### 3-1-9. SP-LP Switching Circuit

The SP-LP switching circuit, consisting of Q706, Q718, and Q719, changes the playback time constant and the frequency response at treble frequencies depending on the tape format. Details of operation are as follows.

In the β Format VCR, the SP (short play), or the βII format, mode of operation and the LP (long play), or the βIII format, mode of operation are different in the playback time constant. In the LP mode of operation, the recording response is reduced as the frequency is high in the treble range. It, therefore, must be compensated for. The Servo Circuit feeds to the SP-LP switching circuit the low-level signal in the SP, or the βII format, mode of operation or the high-level signal in the LP, or the βIII format, mode of operation. In the LP mode of operation, the high-level signal turns Q706 on, which connects the series circuit of C709 and R717 to the playback compensating negative feedback circuit.

In the SP mode of operation, Q718 is off, collector voltage is high, turning Q719 off. In the LP mode of operation, Q718 is turned on. Its collector voltage becomes low, which turns Q719 on. This connects C732 to the recording compensating circuit described previously. The base of Q718 is connected to the playback +B through resistor R793. In the playback mode of operation, it turns Q719 on. This eliminates switching noises caused in the playback mode of operation.

### 3-1-10. Switching Noise Eliminating Circuit

The switching noise eliminating circuit, consisting of Q716, Q717, and D709, which prevents shock noises from being caused when the electronic switch in the V-8000 changes it's mode of operation. The circuit, also, prevents such possible shock noises from erroneously activating the AGC circuit. Details of operation are as follows.

The emitters of Q716 and Q717 are connected to the respective inputs of the output amplifier and recording amplifier described previously. The +B voltage is differentiated by C725. The differentiated signal is connected to the bases of Q716 and Q717 through resistor R774. If the VCR power is turned on or off, this turns both Q716 and Q717 on, which grounds the noise signal caused in the preceding stage to eliminate it. The playback +B voltage passes D709 and also is differentiated by C724 and C718. The differentiated signal is connected to the bases of Q716 and Q717 through resistor R772. These are turned on upon switching to the playback mode of operation. They, then, ground the noises caused in the preceding stage to eliminate it.

### 3-1-11. Erase Oscillator Circuit

This circuit produces a 50 kHz or 60 kHz erasing signal for use for the bias in the audio head recording or audio dubbing, the erasing current in the audio erasing head recording or audio dubbing, or as the erasing current in the full-width erase head recording. The oscillation frequency in recording is determined mainly by a resonant circuit comprised of the full-width erase head, audio erase head, C739, and C742. The one in audio dubbing is determined mainly by a resonant circuit comprised of the audio erase head and C739. C740 and C741 are connected in parallel with C742 by a Fasten tip.

The Fasten tip is to be selected to make equal the erase oscillation frequency in audio dubbing and the one in recording.

In audio dubbing, Q721 turns off as the recording +B voltage is not applied to its base through resistor RM04. The erase oscillation signal, is rectified through D702 and is charged in the capacitor formed of the shielding wire between pins 3 and 4 on the terminal P702. This prevents current from flowing to the full-width erase head in the whole cycle of the oscillation signal.

In recording, Q721 turns on as the recording +B voltage is applied to its base through resistor. The erase oscillation signal is then, rectified through D706, however sine-wave erase current flows to the full-width erase head as a parallel resonant circuit formed of the full-width erase head and C742 resonates at the erase oscillation frequency.

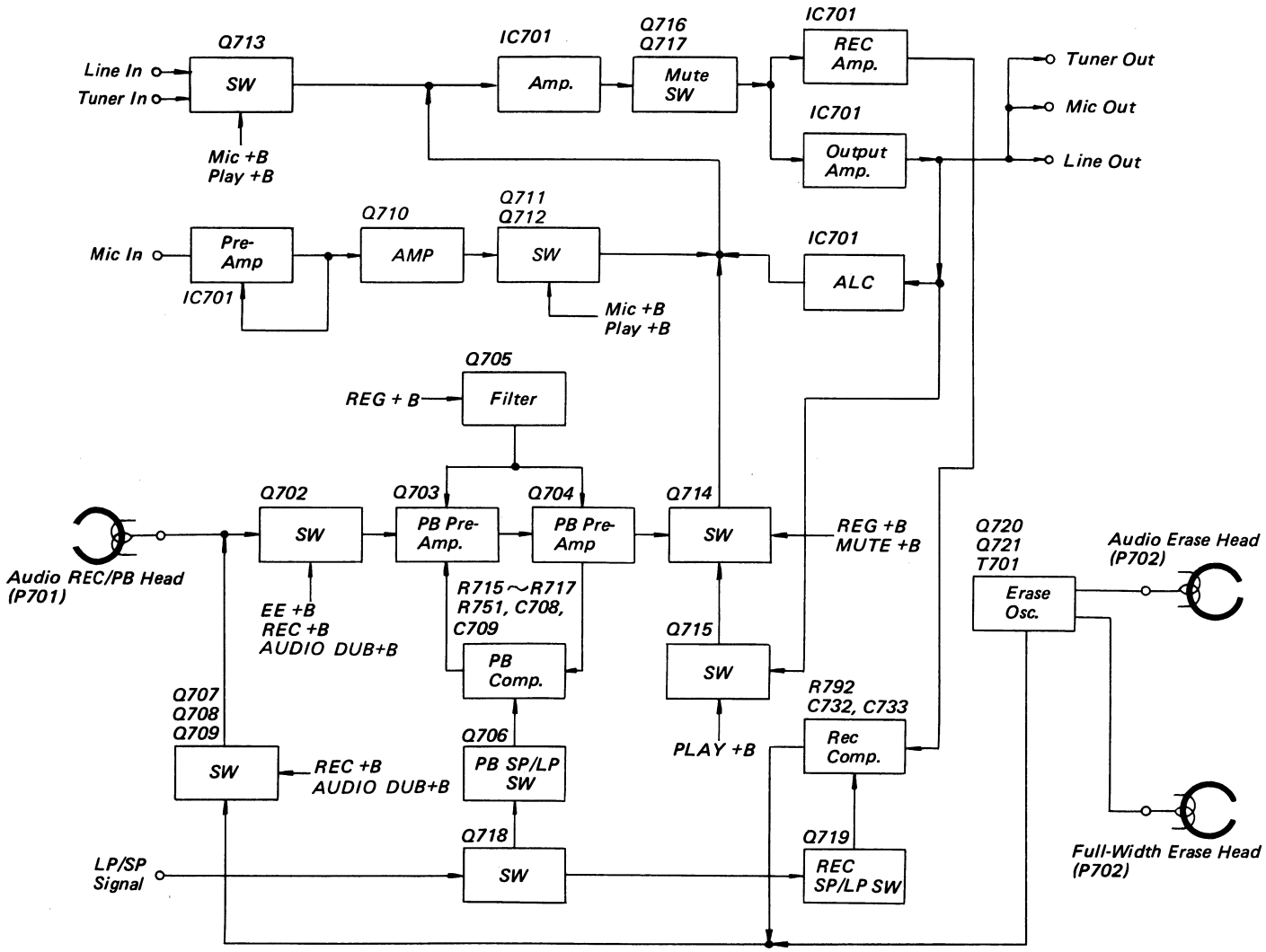



**Fig. 3-72 Audio Circuit Block Diagram (PW2231)**

## 4-1. PROGRAM TIMER SYSTEM

### 4-1-1. General

The Program Timer Circuit consists of a single microcomputer chip (TM4315AP-0403), and it has features that it is capable of being preset for programming recording instants of time in one week to periodically record only a single series of either daily or weekly programs.

The clock in the circuit is made up in a digital fashion. It makes use of the power frequency as the reference frequency. Its timer has LEDs (light-emitting diodes) of dynamic activation type.

The Program Timer Circuit can be preset to record a desired series of either daily (everyday) or weekly (every week) programs by setting a timer-started operation instant of time in the day of the week, hour, and 10-minutes, and minutes, and also contains a timer-set operation period of time in hours and minutes. It, also, can be preset for "sleep recording" by which recording is automatically stopped in time by setting the timer-set operation period of time only.

### 4-1-2. Clock

The clock shows a current time within 12-hours AM or PM in a digital fashion. It, also, indicates the day of the week in a way that the corresponding LED illuminates. As the clock uses the power frequency as its reference, the frequency selector switch SX89 must be set to the position of the frequency, 50 Hz or 60 Hz, in a region where the VCR is used.

### 4-1-3. Interruption Indication

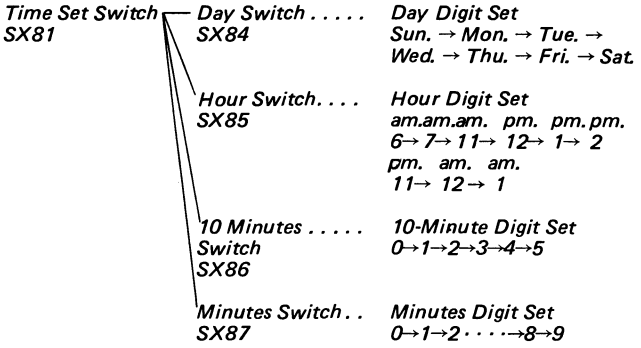
Insertion of the power plug of the VCR into a wall outlet supplies power to the Program Timer Circuit, which starts operation. Such a power application resets the microcomputer at the leading edge of the power voltage. The readout flashes indicating "SUN" and "AM 6:00". Flashing, also, occurs after a service interruption, and the power is recovered. Such an interruption indication stops when the current time is entered and the clock starts.

### 4-1-4. Entering the Current Time

To enter the current time into the Program Timer Circuit, Proceed as follows.

1. Hold the TIME SET button SX81 pressed.
2. Press the DAY button SX84, HOUR button SX85, 10-MINUTE button SX86, and MINUTE button SX87 in the sequence until the current time is correctly entered.

**NOTE:** There are two buttons which are used for the minute setting, SX86, and SX87.
SX87, sets the least significant digits which go from 0 – 9.
SX86, sets the higher digits which go from 0 – 5.




*NOTE: Each time digits circulate, the upper digits is not incremented.*

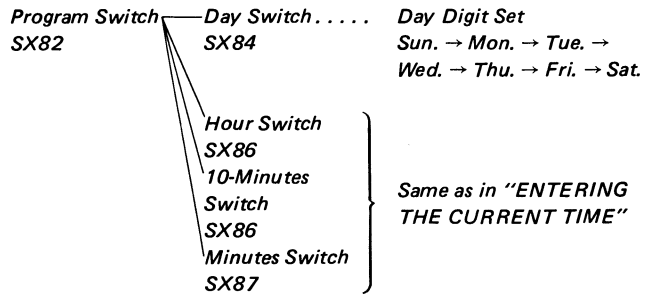
3. While holding the TIME SET button SX81 pressed, the clock stops and is reset at "0" sec. Release the button when a radio time-signal is heard. The clock starts with "0" sec.

**NOTE:** The time digits are advanced one step with every depression of the button. It can be fast-advanced by continuously pressing the button.

### 4-1-5. Entering Timer-Started Operation Time

To enter a desired start recording time into the program timer circuit, proceed as follows.

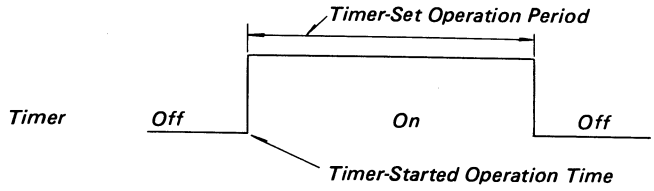
1. Hold the PROGRAM button SX82 pressed.
2. Press the DAY button SX84, HOUR button SX85, 10-MINUTE button SX86, and MINUTE button SX87 in the sequency until the desired start operation of time is entered.




*NOTE: For the every day (daily) indication, all day digit LEDs go out.*

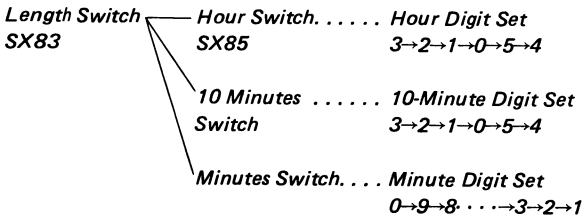
### 4-1-6. Entering the Timer-Set Operation

The Program Timer Circuit can have up to 5-hours 59 minutes entered as the recording period of time. To enter into the Program Timer Circuit a desired operation period of time between the recording start time and end time, proceed as follows.



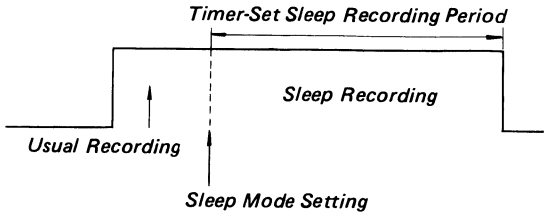

1. Hold the LENGTH button SX83 depressed.
2. Press the HOUR button SX85, 10-MINUTE button SX86, and MINUTE button SX87 in sequence until the desired period of time is entered.

**NOTE:** The day of the week that is stored in the circuit is the one in the timer-started operation time.



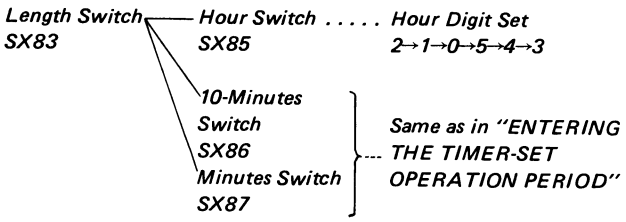

### 4-1-7. Sleep Recording

The "sleep recording" is an operation that when the VCR runs in the recording mode, the VCR is automatically turned off to stop recording in a designated time.



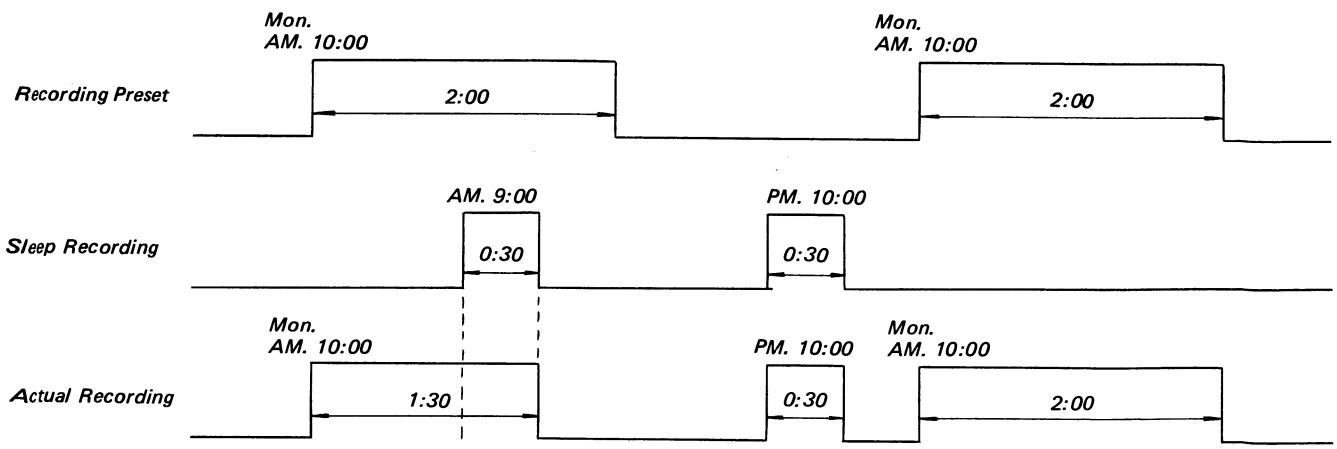

To set the VCR in the sleep recording mode of operation, proceed as follows.

1. While holding the SLEEP button SX88 pressed, set the POWER/TIMER switch SX01 to the TIMER position. This forcibly prompts the Program Timer Circuit to start working.
2. Enter a desired sleep recording period of time in the same way as was used in the timer-set operation period (refer to Section 4-4-6 above).




When the preset sleep recording time elapses, the VCR is turned off.

It should be noted that the sleep recording has higher priority than the timer-controlled operations, which is illustrated below. The sleep recording, however, does not erase the timer-started operation time and timer-set operation period. These remain stored in the Program Timer Circuit. If the POWER/TIMER switch SX01 is held in the TIMER position, the Program Timer Circuit starts working again when the period of time entered in the circuit elapses.



## 4-1-8. Circuit Description
### 4-1-8-1. Time Setting Circuit

The time setting circuit detects the input signal in a time division way. If the scan signal output of pin-27 on ICX01 is a high level, this turns QX08 off, which turns QX09 on. This allows reading the input signals to switches SX84, SX85, SX86, and SX87 only. If the scan signal is a low level on the other hand, this turns QX08 on, which turns QX09 off. This allows reading the input signals to switches SX01, SX81, SX82, and SX83 only. That is, a single scan signal and four input pins are used for reading the input signals to the eight switches.

| Pin 27 Scan | Pin 2 K1 | Pin 3 K2 | Pin 4 K3 | Pin 5 K4 | Switches |
|---|---|---|---|---|---|
| H | H | L | L | L | SX88 Sleep Set |
| ↓ | L | H | L | L | SX85 Hour Set |
| | L | L | H | L | SX84 Day Set |
| | L | L | L | H | SX86 10-Minutes Set |
| L | H | L | L | L | SX01 Timer Mode Set |
| ↓ | L | H | L | L | SX81 Time Set |
| | L | L | H | L | SX82 Program Set |
| | L | L | H | H | SX83 Length Set |

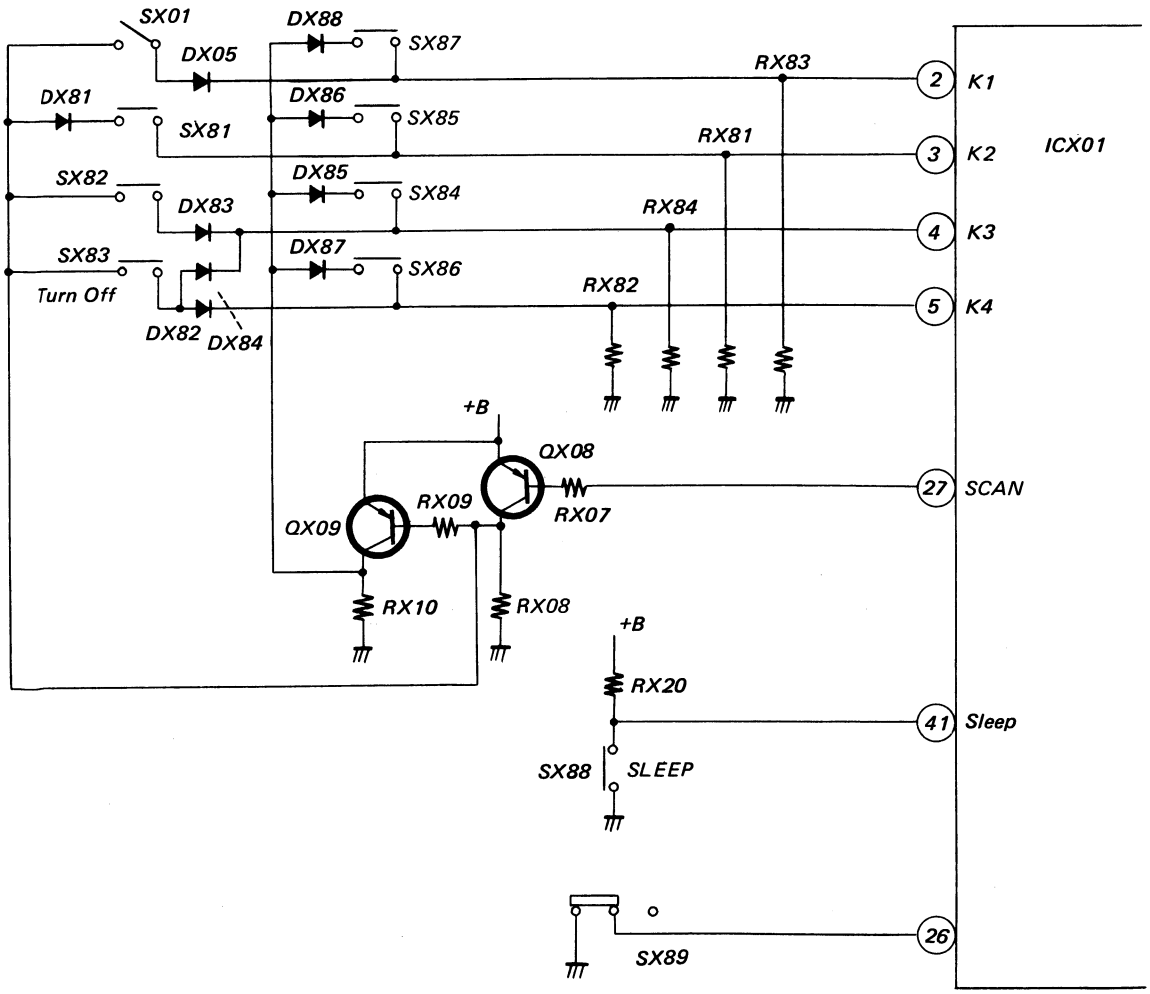



**Fig. 4-73 Time Setting Circuit**

### 4-1-8-2. Time Readout Circuit

The time readout displays current time in a 1/5 duty sequential dynamic activation way using segment signals from pins 10, 11, 12, 13, 31, 32, 33, and the digit selection signals from pins 6, 7, 8, 9, and 18.

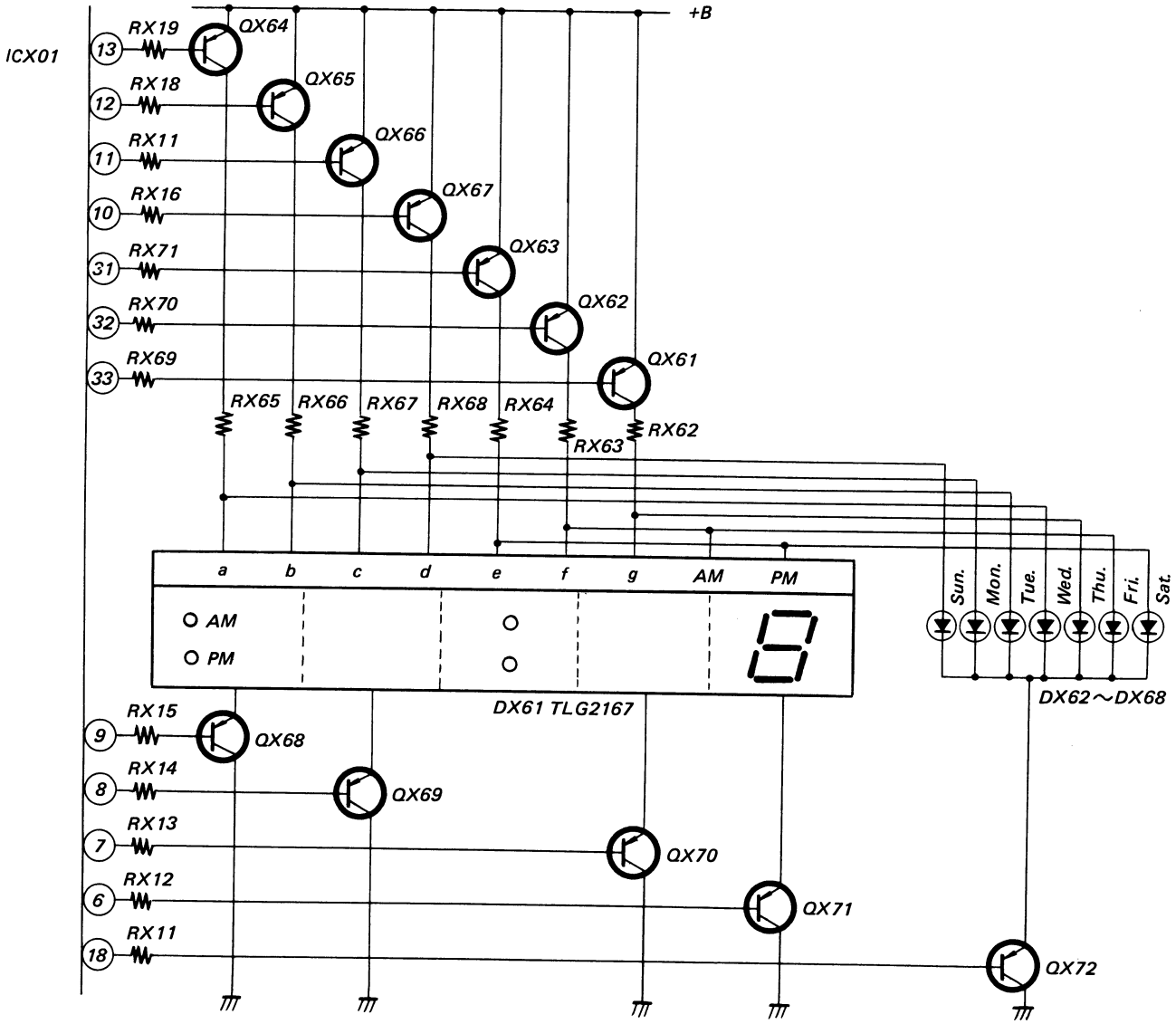



**Fig. 4-74 Time Readout Circuit**

### 4-1-8-3. Reset Circuit

The reset circuit functions to stop the microcomputer operation if the +B voltage supplied to the Program Timer Circuit drops down by some cause, for example, service interruption. The reset circuit, also, can start the Program Timer Circuit from the reset initial state if the +B voltage is recovered to the normal value.

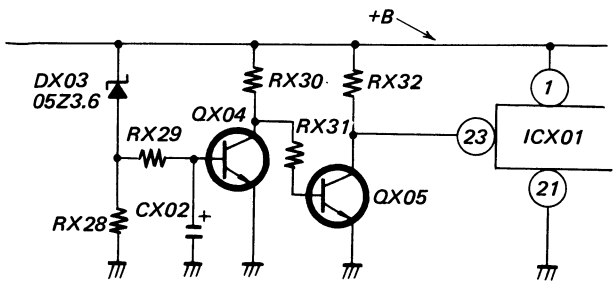



**Fig. 4-75 Reset Circuit**

In the figure, if the +B voltage supplied to the Program Timer Circuit drops lower than $V_Z + V_{BE}$ where $V_Z$ is the zener voltage of DX03 and $V_{BE}$ is the voltage between the base and emitter of QX04, the low +B voltage turns QX04 off. The result is that the microcomputer operation stops.

If the +B voltage at pin-1 on ICX01 rises up by removal of the cause to voltage-down, for example, with the recovery of the line voltage, it may reach higher than $V_Z + V_{BE}$.

Then, DX03 starts conducting. The integrating circuit, consisting of RX29 and CX02, keeps the voltage at pin-23 at 0 V until CX02 is charged to a voltage higher than $V_{BE}$. This assures that the microcomputer is reset to the initial state before the Program Timer Circuit starts.

### 4-1-8-4. Reference Signal Input Circuit

The reference signal input circuit converts to a form to input into the microcomputer the power frequency, 50 Hz or 60 Hz, which is used as the reference to the operation of the clock. It uses a Schmitt trigger circuit, consisting of QX02 and QX10 as shown in the figure below.

The Schimitt trigger circuit has the input signal to which the 50 Hz or 60 Hz voltage has been half-wave-rectified in the Power Supply Circuit. It shapes the input signal to a proper form to prevent an undesired interference or noise signal from affecting the reference signal for the clock.

### 4-1-8-5. Timer Output Circuit

The timer output circuit, which is interlocked with the POWER/TIMER switch, controls power on-off the VCR upon the starting operation of the Program Timer Circuit. At the same time, it controls the electronic Logic Control Circuit so that this may set the VCR into the recording mode of operation upon the starting operation of the Program Timer Circuit.

In the figure, if the POWER/TIMER switch is in the OFF position, the switches SX01-A and SX01-C are open. These allow turning on the switching transistor Q813 in the Power Supply Circuit which turns off the VCR. If the switch is in the ON position, on the other hand, switch SX01-A is closed. This turns Q813 off which turns the VCR on.

If the switch SX01-C is closed, the VCR is in the timer-controlled mode of operation. If the Program Timer Circuit is not activated, then, pin-19 on ICX01 is at a high level. This turns QX06 off, which turns QX07 off. This allows the bias voltage to flow thru RX03 to Q813. Thus, Q813 holds the VCR turned off. On the other hand, if the Program Timer Circuit is activated, then, pin-19 is at the low level (0 V). This turns QX06 on, which turns QX07 on. This turns QX813 off, which turns the VCR on. At the thru time, bias is applied through DL32 and RL30 to QL21. This electrically sets the VCR in the recording mode of operation.

The diode DX08 and the resistor RX02 operate as follows, if the switch SX01-C is open, it serves to lower the bias voltage at the base of QX07 which holds it off. If SX01-C is closed, on the other hand, the voltage across RX02 becomes approximately 3 V, which does not allow DX08 to conduct. This makes QX06 control the bias at the base of QX07.

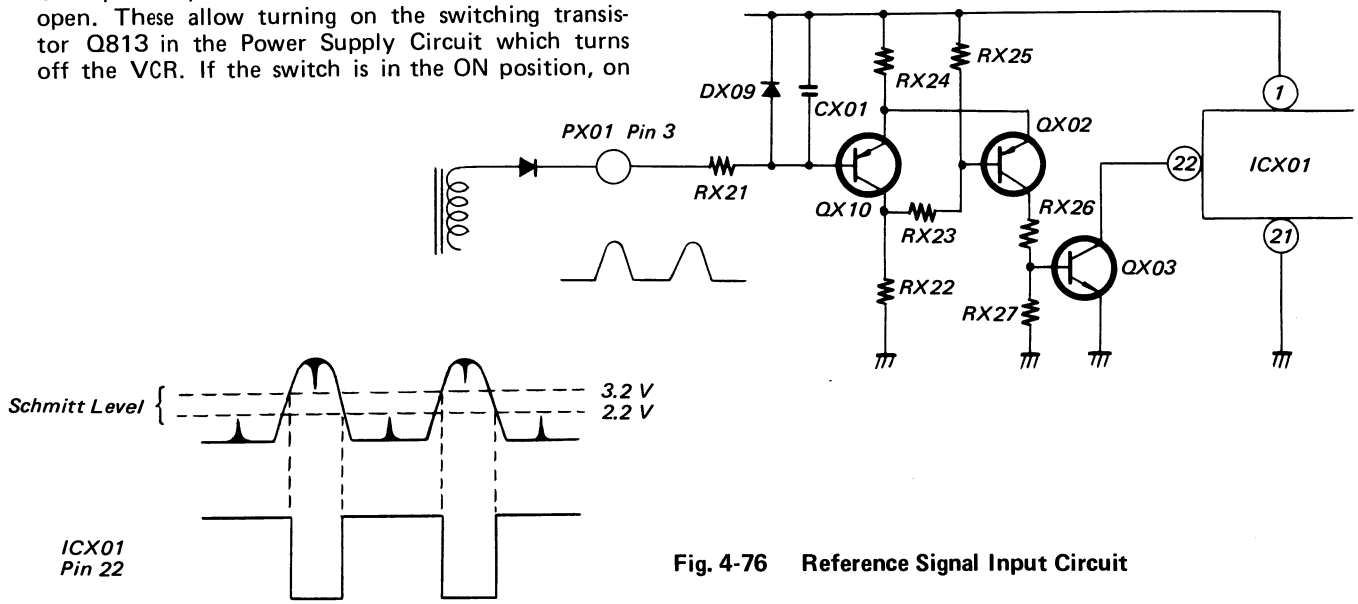



Fig. 4-76 Reference Signal Input Circuit

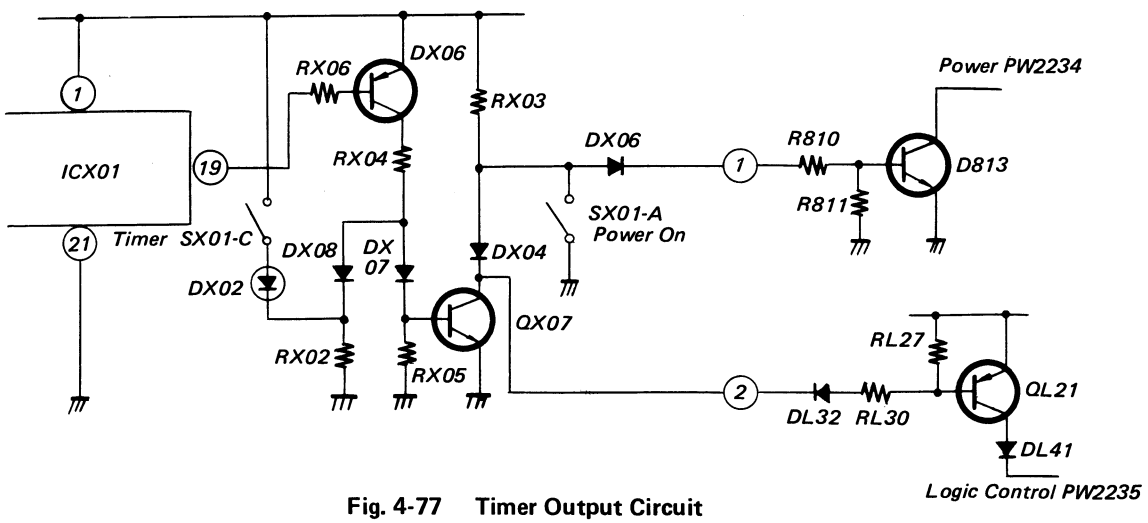



Fig. 4-77 Timer Output Circuit

## 5-1. TUNER SYSTEM

### 5-1-1. General

The Tuner Block consists of an Antenna Terminal Board, a Tuner, a Selector Circuit, a PIF and SIF Circuit, and a Modulator Circuit. The operation of the Tuner Circuit is as follows.

The incoming signal induced in the VHF or UHF antenna is converted to stable video and audio signals. Instead, the signal from a Video camera or similar video equipment may be fed to the Video and Audio Circuits. In the playback or monitoring mode, the signals of the Video and Audio Circuits, may be either fed out directly to video equipment, such as monitor TV set, or converted to composite TV signal (RF wave) in a low VHF channel to receive by a usual TV set.

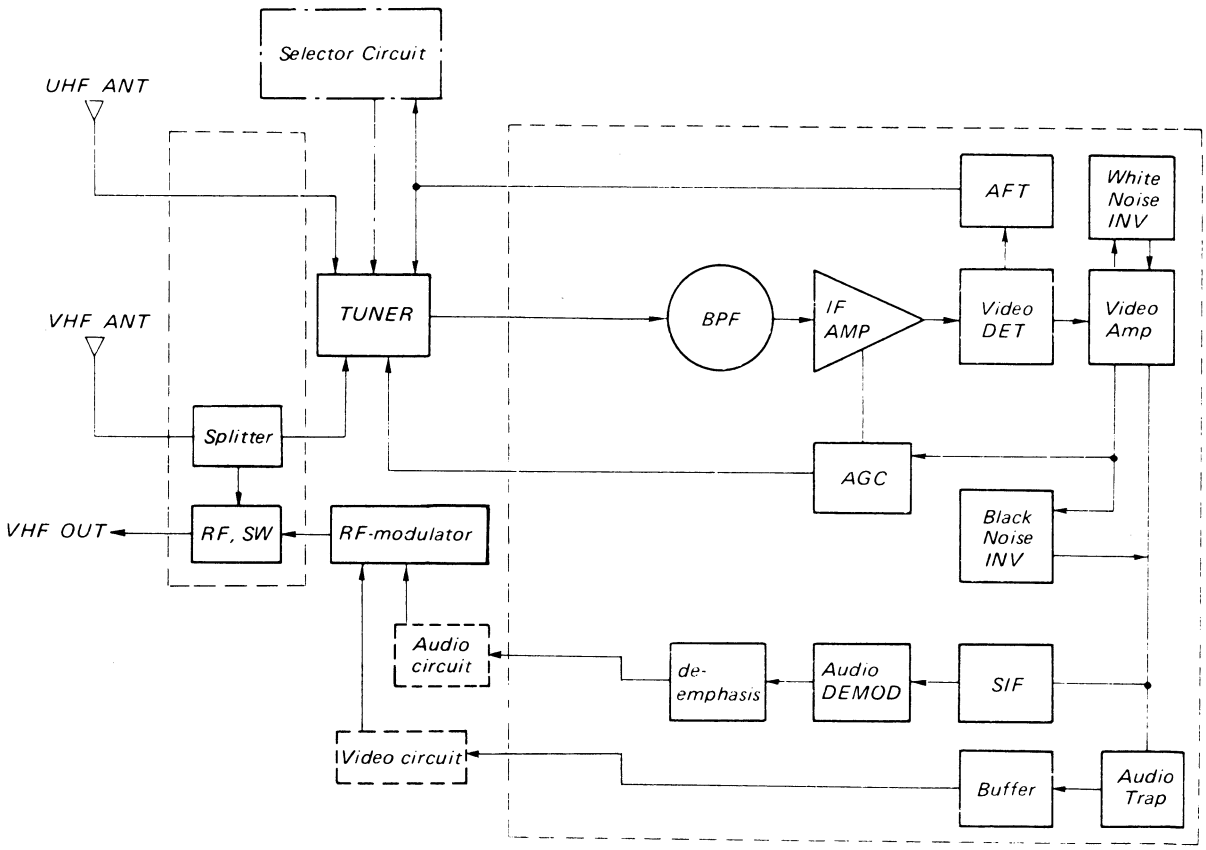



**Fig. 5-78 Tuner Block Diagram**

### 5-1-2. Antenna Terminal Board

The Antenna Terminal Board is not involved in the UHF signal input as this passes through the board only.

In the circuit shown in Fig. 5-79, the RF siganl induced in the VHF antenna passes the high-pass filter, consisting of L1, L2, and C1, to the balance and unbalance transformer T1. The balance and unbalance transformer splits the signal into two parts, the one of which is fed to the Tuner on the VCR and the other to the RF switch through C4

The 5 V +B line is live even if the POWER/TIMER switch is in the OFF position. Note that it, also, is used as the power source for the Program Timer Circuit.

The power source at pin-3 on P605 on the Servo and Logic Circuit board is selectively set to 10 V when the TV/VCR antenna switch SL11 is in the VCR position, or to 0 V when the switch is in the TV position. The power source, also, is set to 10 V when the PLAY button is pressed. Note that it is 0 V when the POWER/TIMER switch is in the OFF position.

If the POWER/TIMER switch is in the OFF position or the TV/VCR antenna switch is in the TV position, the power source at pin-3 on P605 is 0 V as mentioned above. The diodes D1 and D3, then, are on and D2, D4, and D5 are off. The RF signal coming from C4 passes D1, D3, and C9 to the VHF OUTPUT terminal, to which it is sent to the TV set. Note that the power source for the RF modulator is turned off to keep improved isolation.

On the other hand, if the TV/VCR antenna switch is in the VCR position or the PLAY button is pressed, the power source at pin-3 on P605 is 10 V as mentioned previously. The diodes D2, D4, and D5, then, are on and D1 and D3 are off. This allows the RF modulator to feed its output RF signal through C10, D5, and C9 to the VHF OUTPUT terminal, from which the RF signal is sent to the TV set.

The operations of the VCR and TV selected by the operating switches and TV/VCR switch are charted in the table 5-14.

For instance, even if the TV/VCR antenna switch is in the TV position, the VCR is powered on to operate by pressing the PLAY button. It should be noted that if the TV/VCR antenna switch is pressed during playback, either TV or VCR can be selected to operate. If the STOP button is pressed, in turn, this holds the operation mode set by the TV/VCR antenna switch during playback.

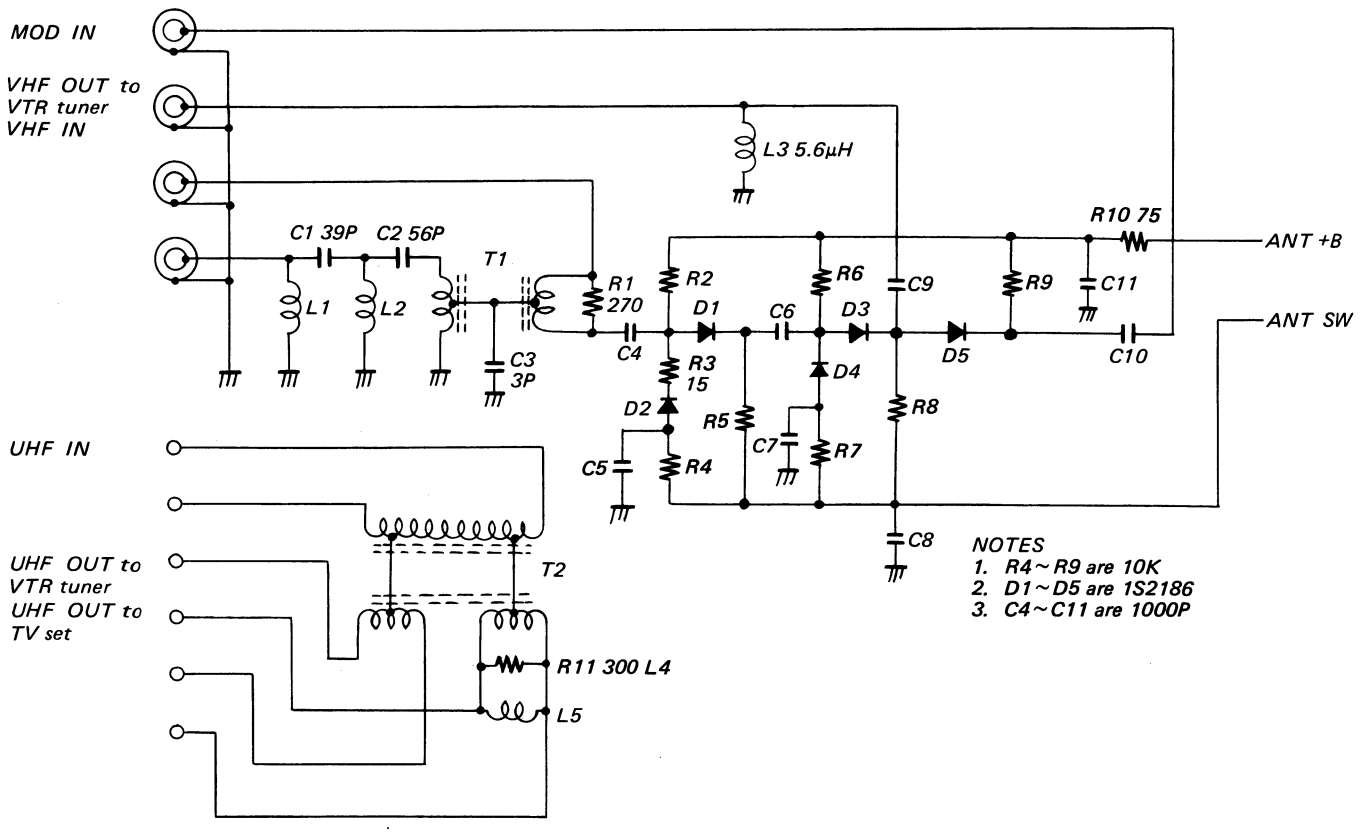



**Fig. 5-79 Antenna Terminal Circuit**

| MODE OF OPERATION | TV/VCR SW POSITION | |
|---|---|---|
| | TV side | VCR side |
| Playback | VCR | VCR |
| Recording | TV | VCR |
| Audio dubbing | TV | VCR |
| Stop | TV | VCR |
| Power-off | TV | TV |

**Table 5-14**

### 5-1-3. Electronic Tuner, PIF, and Selector Circuit

#### 5-1-3-1. VHF Tuner Section

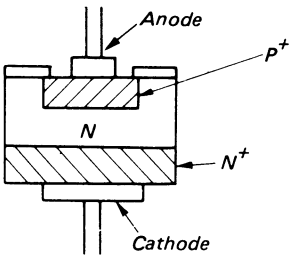



**Fig. 5-80 Varactor Construction**

The varactor, as illustrated in Fig. 5-80, is a PN junction diode characterized by a voltage-sensitive capacitance. In the figure, P+ is a region where a trivalent impurity is doped in bulk, and N is a region where a pentavalent impurity is doped little. If a reverse bias is applied to the varactor, or if a negative voltage is connected to the anode and a positive voltage to the cathode, an electric double layer called the "depletion layer" having no mobile carrier charge is forward at the junction between P+ and N. The capacitance of the imaginary capacitor formed by the charges of the depletion layer can be varied as a function of the reverse bias.

The equivalent circuit of the varactor is shown in Fig. 5-81. In general, RN > Rp + and RN > RN+. Also, RN is high with the capacitance. The varactor made of silicone variable in the capacitance from 2 pF (30 V) to 12 pF (3 V) has RN around 0.5 Ω at maximum. A usual variable capacitor, the equivalent circuit of which is represented by C and R in series, has R around 0.01 Ω involved mainly in the rotor contact. Such a high RN as compared with R of the variable capacitor is one of most important difficulties affecting the characteristics of the varactor, particularly in inhibiting high Q of the tuning circuit. High sensitivity cannot be obtained by the tuning circuit, but a proper NF and gain are obtained.

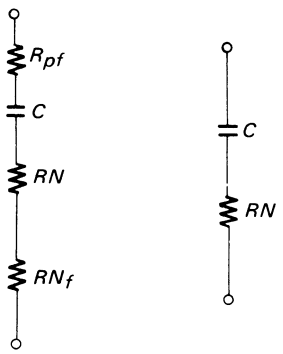



**Fig. 5-81 Varactor Equivalent Circuit**

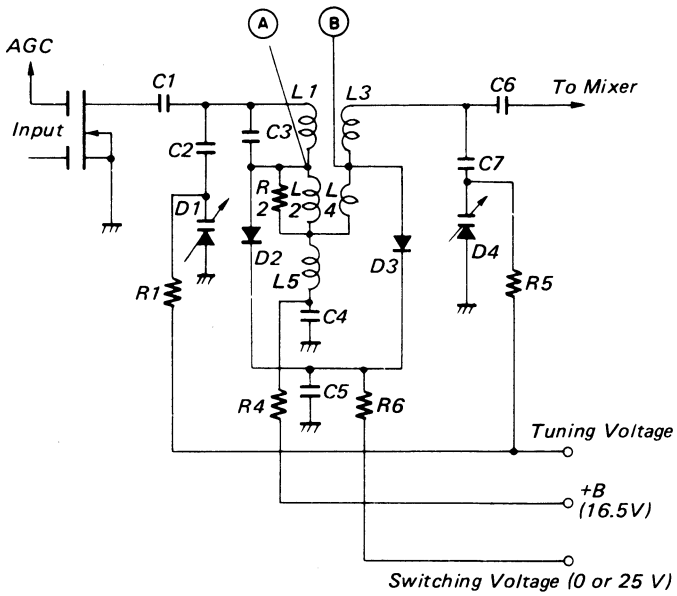



**Fig. 5-82 Tuning Circuit**

In the following is described the tuning circuit of the Electronic Tuner with respect to the interstage tuning circuit of the EL311 as an example. In Fig. 5-82, if the switching voltage is 0 V, a loop is formed, which allows current to flow from the +B source through R4, L5, L2, L4, and R6. The current applies forward bias to D2 and D3, which conduct. This means that points A and B are grounded by C5 to form a tuning circuit of D1, C2, C3, and L1. This circuit can be tuned into a high channel with capacitance changes of the varactors D1 and D4 by the tuning voltage. If the switching voltage is 25 V, on the other hand, D2 and D3 are reverse-biased, which do not conduct. In this state, an additional circuit, consisting of L2, R2, L4, and L5, is placed the tuning circuit, which tunes into a low channel. The resistor R2 serve for damping the tuning sensitivity of the coil.

As described above, the varactor capacitance variable range is too narrow to cover all channels. In general, therefor, switching diodes are used together with the varactors for tuning into any of low and high channels. It should be noted that the Tuner EL311 is installed on the Selector Circuit board.

#### 5-1-3-2. UHF Tuner Section

As described in the preceding section, the Q of the varactor is far lower than that of the variable capacitor. To overcome such a deficiency, an additional input RF amplifier is provided in the Electronic Tuner. Also, an additional IF amplifier is placed behind the mixer and the output of the UHF tuner section is connected to the input of the VHF mixer to make the gain in the UHF band coincide with the one in the VHF band.

### 5-1-3-3. PIF Circuit

The IF signal entered from EL311 on the Selector Circuit board PW2229 is amplified around 18 dB by the ground-emitter IF amplifier Q001. L001 and R001 are placed to make the input impedance to 75Ω at the center frequency fo to minimize response change due to the IF cable. L002 is tuned at a frequency with the input capacitance of the surface acoustic wave filter, which will be described in the following paragraphs, to make the IF amplifier frequency response rather flat. Q003 blocks the flow of the DC current to the surface acoustic wave filter. The IF amplifir is placed to compensate for the insertion loss of the surface acoustic wave filter.

The surface acoustic wave filter services to pass the signal in the IF band, to trap the signals in the adjacent channels 1.5 MHz above and 6 MHz below the picture carrier frequency, and also to trap the audio signal at 4.5 MHz below. The surface acoustic wave filter needs no alignment and is improved in the reliability and reduced in the number of parts used as compared with the conventional filters comprised of inductors and capacitors.

The surface acoustic wave is similar to the wave propagation caused on water surface, such as a pond, when a stone is thrown in. The surface acoustic wave propagates on the boundary between an elastic and air, or on the surface of the elastic.

The surface acoustic wave filter is illustrated in Fig. 5-83. As shown in the figure, an input and output inter-digital transducers are put on piezoelectric substrate. If a AC voltage is applied to the input transducer, an AC electric field is produced between the electrodes of the input transducer on the surface of the substrate. The electric field causes a mechanical expansion and contraction, or an elastic strain. The strain energy is concentrated and propagates rightly under the surface of the substrate. The propagating waves are summed up and received by the output transducer.

The propagation velocity of the surface acoustic wave denoted by Vs is determined in terms of the substrate characteristics and crystal structure. The amplitude is in proportional to the strength of the electric field produced by the input voltage and of the distance between the two transducers. The center frequency denoted by fo is given by

$$fo = \frac{Vs}{\lambda}$$

where $\lambda$ is the interval of the inter-digits of the transducer. The amplitude of the surface acoustic wave produced by a pair of opposite digits is in proportion to the interpolation of the digits. The phase of the acoustic wave depends on the positions of the digits.

The bandwidth of the filter is narrow and the impedance is low with increase of the number N of pairs of opposite digits as this increases the stress by signals around the center frequency. The frequency response of the product of those of the two transducers, or the exciting (input) transducer and receiving (output) transducer. If the receiving transducer has a few interdigits, the frequency respone of the filter depends to a high degree on that of the exciting transducer.

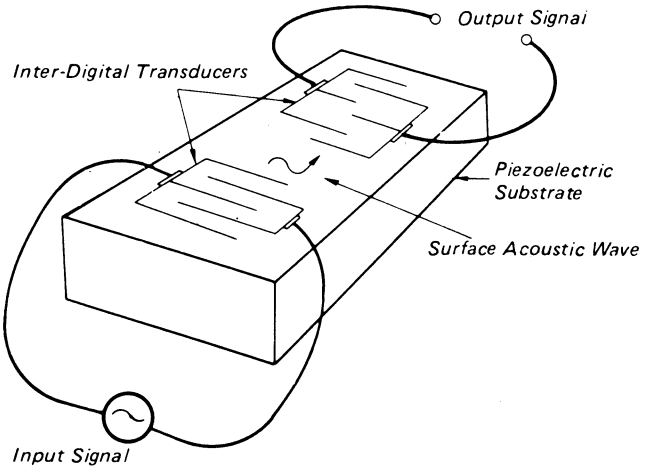



**Fig. 5-83 Surface Accoustic Wave Filter Structure.**

The surface acoustic wave filter (hereinafter referred to as "PSF filter") is designed so that its center frequency should be around 45 MHz and the bandwidth is selected to minimize the adjacent video and audio frequency responses. These are achieved by properly determining the interval and number of the digits of the exciting transducer and by making flat the frequency response of the receiving having a few digits.

As shown in Fig. 5-84 below, the signal passed the PSF filter enters pins 1 and 16 on IC002 (TA7607AP) and is magnified 57 dB by the IF amplifier, consisting of three differential amplifier stages. The IF amplifier can be gain-controlled up to 63 dB as a succeeding stage controls the gain of the preceding stage in sequence, thereby providing good signal-to-noise ratio. The IF amplifier, also, has a DC feedback from the output to the input to minimize undesired offset in the differential amplification.

The amplified PIF-signal is taken out and routed by the emitter follower into the "and" circuit, or the multiplier, and through the other emitter follower the differential amplifier having the 45.75 MHz tuning network and limiter as loads. The limiter restricts the signal to produce the video carrier of a constant amplitude. The video carrier is led as a switching signal to the "and" circuit. The "and" circuit homodyne-detects the video signal from the PIF signal with use of the switching signal. The video signal is magnified by the grounded-base amplifier and is fed out through the emitter follower.

Also, the switching signal is divided into two parts: one is directly led to and the other through an external 90° phase shifter to the other "and" circuit. This "and" circuit produces a DC voltage that corresponds to the frequency difference between the two signals. The DC voltage is magnified for use as the AFT voltage.

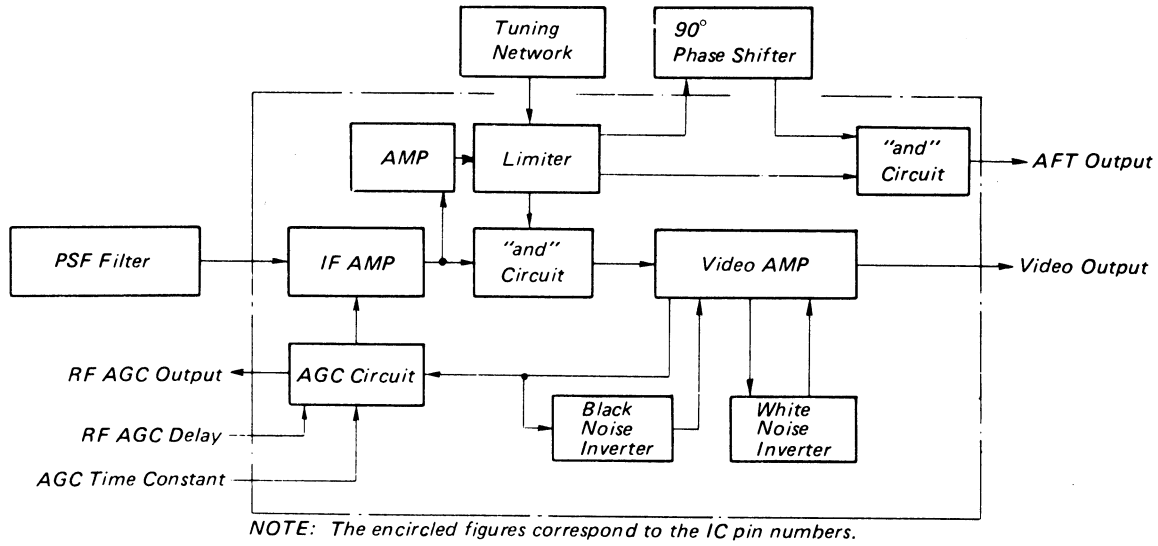



**Fig. 5-84 PIF IC (TA7607AP) Block Diagram.**

In addition to the above-mentioned functional circuits, the PIF IC (TA7607AP) contains a black noise inverter and white noise inverter that cut out undesired noises to clamp to certain levels as illustrated in Fig. 5-85.

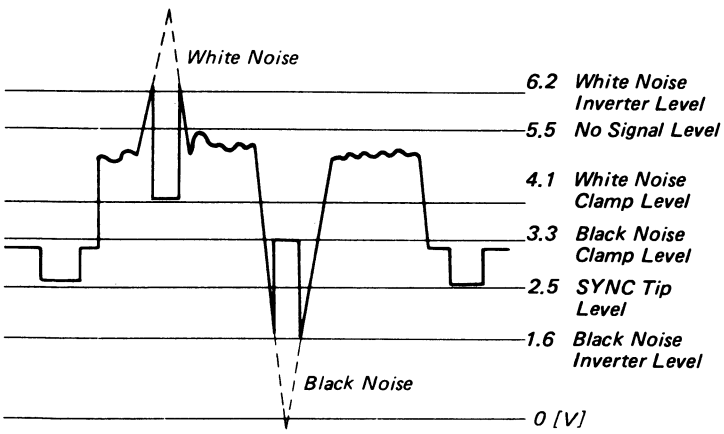



**Fig. 5-85 Noise Clamp Levels.**

The video signal fed out from pin 12 of the PIF IC is divided into two parts: one passed the 4.5 MHz audio trap to eliminate the audio signal and is output by the emitter follower having 75Ω output impedance; and, the other passes the 4.5 MHz ceramic bandpass filter and is fed to the Audio Detection IC003 (TA7176AP). In the Audio Detection IC, the SIF signal is limited and amplified by three differential amplifier stages and passes the low pass filter which eliminates the harmonic components to improve the AM suppression ratio. The SIF signal, in turn, is divided into two routes: one is directly connected to the input of the differential amplifier and the other to the phase shifter, comprised of a ceramic filter, where the signal is phase-shifted 90° and also is fed into the differential amplifier. As the SIF signal is deviated from 4.5 MHz, the signal passing the phase shifter deviates more than 90°. This deviates the turn-on and turn-off periods of time, that is, the audio signal is frequency detected.

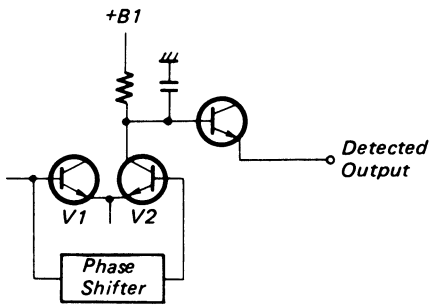



**Fig. 5-86 Differential Amplifier Circuit.**

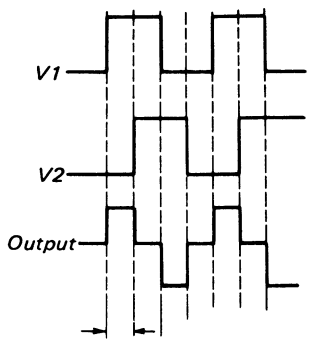



**Fig. 5-87 Differential Amplifier Time Chart**

### 5-1-3-4. Selector Circuit

The Electronic Tuner, as described the "VHF Tuner Section", is controlled by DC voltage to tune into a desired channel. If the DC voltage is stored for each channel, the tuner can be turned into it at any time by depressing the button corresponding to it.

The DC voltage is mechanically memorized by the variable resistor, through which it is sent through the superimposing circuit to the ET Tuner to tune into the desired channel, as illustrated in Fig. 5-88.

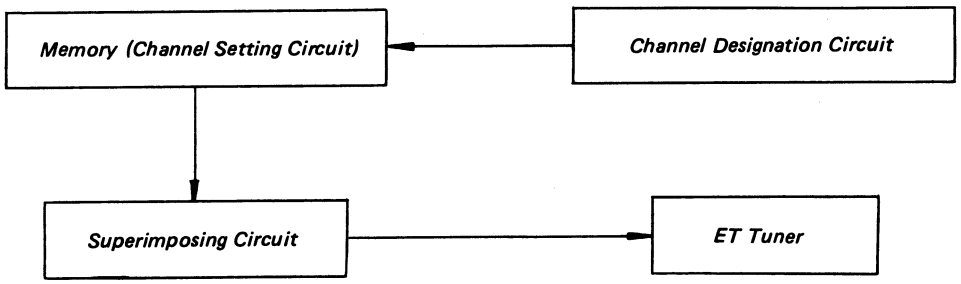



**Fig. 5-88 Selector Circuit Block Diagram.**

## 6-1. POWER SYSTEM

### 6-1-1. General

The Power System consists of a power transformer T802, an AC noise filter circuit, and voltage regulator circuits. These are accommodated in the Line Filter Circuit board PW2230, the Power Supply Circuit board PW2234, and the Power Drive Circuit board PW2351 are described in Section 6-6-2 below.

### 6-1-2. Power Circuit Boards

The Line Filter Circuit Board PW2230 contains an AC noise filter circuit, 16.5 V and 5 V rectifier circuits, 16.5 V and 5 V voltage regulator circuits, a 12 V differential amplifier circuit, and a heater line switching circuit. The Power Supply Circuit board PW2234 contains a 12 V rectifier circuit, a 45 V rectifier circuit, and voltage regulator circuit, and a power line switching circuit. The Power Drive Circuit board PW2351 contains a 12 V drive circuit and part of a 5 V drive circuit. These functional power circuits will be described in detail in the following sections.

### 6-1-3. Rectifier Circuits

The AC voltage across the secondary winding (P802, pins 3, 5) of the power transformer T802 is bridge-rectified through the rectifier stack to obtain a DC voltage of approximately 19 V. This DC voltage is fed to the 12 V voltage regulator circuit, and the 5 V power drive circuit.

The AC voltage across the tertiary winding (P802, pins 1, 2) is half-wave-rectified through D820 to obtain a DC voltage of approximately 72 V. This DC voltage is fed to the 45 V voltage regulator circuit.

The AC voltage across the quarternary winding (P803, pins 3, 4) is rectified through the bridge of D803 to D806 to obtain a DC voltage of approximately 23 V. This DC voltage is fed to the 16.5 V voltage regulator.

The AC voltage across the quinary winding (P803, pins 1, 2) is rectified through the bridge of D807 to D810 to obtain a DC voltage of approximately 9 V. This DC voltage is fed to the 5 V voltage regulator circuit.

### 6-1-4. 5 V Voltage Regulator

The 5 V voltage regulator circuit is divided into four power sources for: (1) the LEDs in the Program Timer Circuit which are activated when the power plug P801 is inserted into a wall outlet irrespective of the POWER/TIMER switch, (2) the ICs in the Program Timer Circuit, (3) the antenna switching circuit, (4) the ICs in the Servo and Logic Circuit which is turned on or off by the POWER/TIMER switch.

The power source for the LEDs in the Program Timer Circuit is made up of a transistor Q810 and a zener diode D826 to produce 5 V power voltage. Q810 is installed in position on the heat sink provided outside the PW board to dissipate the generated heat.

The power source for the ICs in the Program Timer Circuit is built up of a transistor Q806 and a zener diode D813 to produce a 5 V power voltage to the antenna switching circuit which is powered from the base of Q806.

The power source for the ICs in the Servo and Logic Circuit are built up of transistor Q809 and a zener diode D817 to produce a 5 V power voltage.

### 6-1-5. 45 V Voltage Regulator

The 45 V voltage regulator circuit, consisting of transistors Q811 and Q812, zener diode D823, and resistors R816, R852, and R817, produces 45 V of regulated power.

### 6-1-6. 12 V Voltage Regulator

The 12 V voltage regulator includes two circuits: one, consisting of transistors Q802, Q804, and Q805, zener diode D812, and resistors R805, R851, and R806, which produce the main 12 V regulated power the second circuit consisting of transistors Q801, Q803, and Q805, zener diode D812, and resistors R805, R851, and R806, produce the 12 V regulated power for driving the motor. Note that Q801 and Q802 are installed on the heat sink provided outside the PW board to dissipate the generated heat.

### 6-1-7. Power On-Off Control

The V-8000 is normally powered on or off by transistor Q813, which is activated On or Off by the POWER/TIMER switch. When the POWER/TIMER switch is in the OFF position, current flows through resistor R810 into the base of Q813, which is turned on. This prevents the turn on voltage to be applied to the base of Q811, this preventing the 45 V voltage regulator from supplying the 45 V power. The transistor Q807 in the 16.5 V voltage regulator circuit is not biased when connected through R824 to the 45 V line. The 16.5 V power, also, is not supplied to the line. Similarly, Q803 and Q804 in the 12 V voltage regulator circuit are not biases when directly connected to the 16.5 V line. The 12 V power, also, is not obtained. Further, Q809 in the 5 V voltage regulator circuit for the ICs in the Servo and Logic Circuit is not biased when connected through R809 to the 12 V line. The 5 V power cannot be supplied. On the contrary, when the POWER/TIMER switch is in the ON position, current does not flow into the base of Q813, which is turned off. This allows Q811 to be normally biased. The 45 V voltage regulator, then, is activated to apply the respective regular biases to Q807, Q803, Q804, and Q809. These transistors activate the respective 16.5 V, 12 V, and 5 V voltage regulators.

On the other hand, when the POWER/TIMER switch is in the TIMER position the Program Timer Circuit feeds out signals corresponding to preset times. Each output signal switches Q813 On or Off, which turns the 45 V, 16.5 V, 12 V, and 5 V voltage regulators On or Off, accordingly.

### 6-1-8. 16.5 V Voltage Regulator

The 16.5 V voltage regulator circuit, consisting of transistors Q807 and Q808 and zener diode D815, produces 16.5 V power with use of 12 V line voltage. The output voltage of D815 and the 12 V line voltage are used as reference voltages. In the leading state right after the POWER/TIMER switch has been turned on, the 16.5 V voltage regulator circuit of Q807, Q808, and D815 outputs a voltage of approximately 5 V. This allows the 12 V voltage regulator to produce a voltage of approximately 3 V. This is added to the 5 V voltage output of the 16.5 V voltage regulator circuit. Such a serial operation is repeated until the 12 V voltage regulator output is maintained normally at 12 V. This keeps the 16.5 V voltage regulator circuit normally at 16.5 V.

### 6-1-9. Heater On-Off Control

The V-8000 has a dew preventive heater installed on the cylinder. When the POWER/TIMER switch is in the OFF position or the cylinder motor is not energized, a voltage of approximately 19 V is applied across the heater. The 19 V voltage is obtained in the manner that current is allowed to the base of a transistor Q842, which turns Q842 on, which at the same time, also turns Q841 on.

On the other hand, when the POWER/TIMER switch is in the ON position or the cylinder motor is running, no bias is applied to Q842, which is turned off and at the same time, also turns Q841 off. This prevents the 19 V volts to be applied to the heater.

### 6-1-10. Others

The AC voltage at the secondary winding (P802, pin-3) of the power transformer is rectified through diode D841 to produce a pulsating current, which is supplied to the dew sensor circuit.

Also, the AC voltage at the quinary winding (803, pin-2) is directly supplied to the Program Timer Circuit.

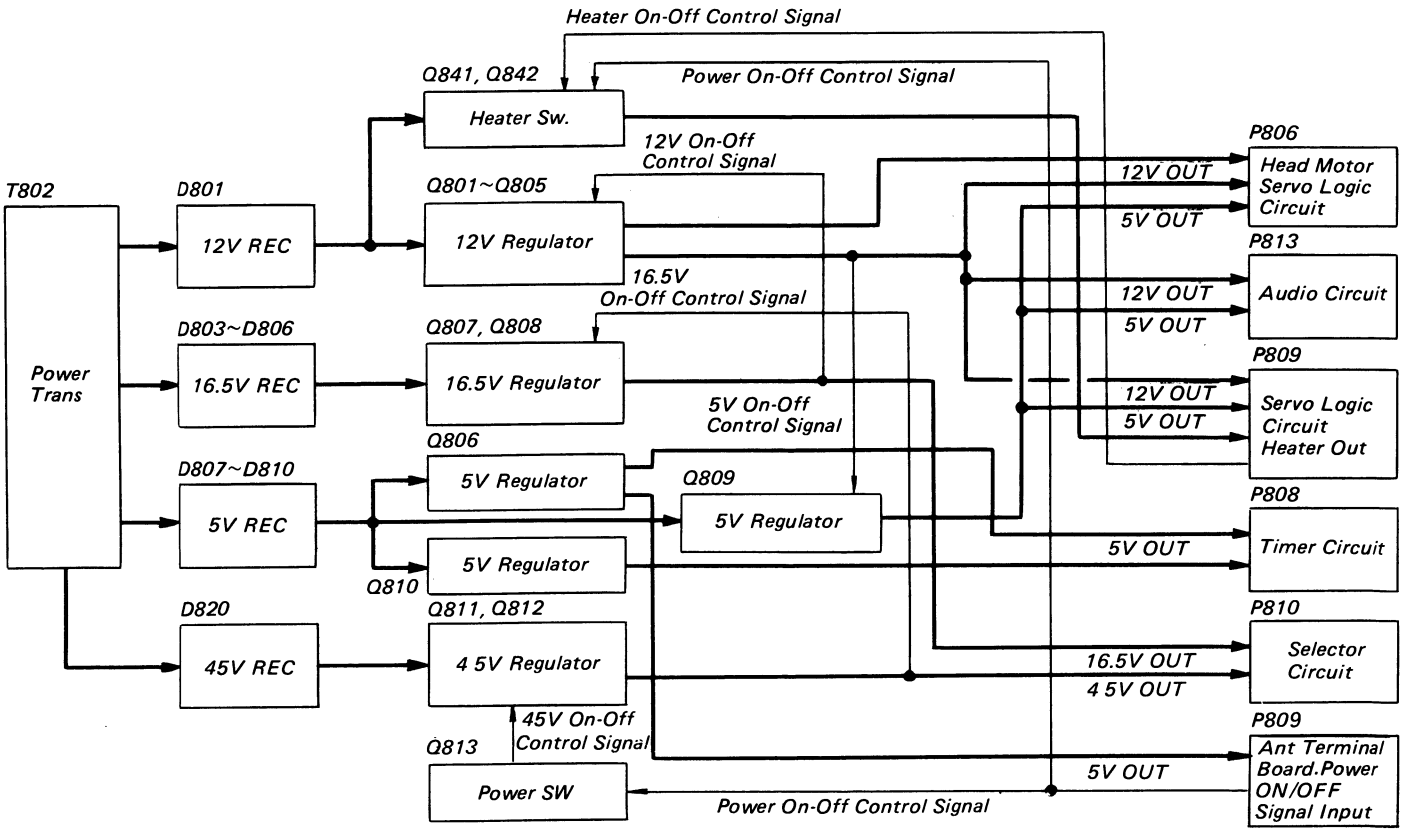



**Fig. 6-89 Power Supply Circuit Block Diagram (PW2230, PW2234, PW2351)**

# SECTION 2 MECHANICAL DESCRIPTION

### 7-1. Tape Loading Operation (see Fig. 101)

The cassette compartment subassembly is locked.

- The locker ① moves downward (↓) and returns back (↑) to lock.
- The cassette detect slider ② moves downward.
- The detect plate assembly ③ and detect lever ④ turn round (↖). The roller of the detect plate assembly.
- ③ detached from the cam way of the loading disk ⑤ . This operation actuates the cassette detect switch ⑥ to turn on.

Tape loading starts.

- The roller of the cam follower plate assembly ⑦ rides onto the cam way on the circumference of the loading disk ⑤ . The roller turns round the cam follower lever ⑧ (↙).
- With the cam follower lever ⑧ turned, the loading slide bar ⑨ moves leftward (←). This operation actuates the supply brake shift lever ⑩ to move upward (↑) along the slope of the loading slide bar ⑨ . The supply brake shift lever ⑩ , then, detaches the supply brake lever ⑪ from the supply reel table ⑫ .
- Similarly, the take up brake shift lever ⑬ is moved to detach the take up brake from the take up reel table assembly ⑮ .
- The roller of the T-type cam follower plate assembly ⑯ is guided by the cam face on the circumference of the loading disk ⑤ to turn the guide lever assembly ⑰ (↖). Turning of the guide lever assembly ⑰ allows the tension spring ⑱ to turn round the tension lever assembly ⑲ to a specified position.

In the course of loading, the pinch roller lever assembly ⑳ is kicked inward two times by the cassette lid opener ㉑ and the pinch roller guide plate ㉒ .

- Right before the end of loading, the roller of the cam follower plate assembly ⑦ reaches the end of the cam face on the circumference of the loading disk ⑤ . The cam follower plate assembly ⑦ , then, returns in the reverse direction (↖). This operation actuates the supply and take up brakes to brake the respective reel tables.

The tab located on the bottom of the loading disk ⑤ is stopped by the stopper on the cylinder base.

- The tab on the bottom of the loading disk ⑤ actuates the loading end detect lever ㉓ to turn around, which turns on the loading end detect switch ㉔ .

The loading motor stops, tape loading is completed.

The play solenoid is energized for a moment to give the tape a slack.

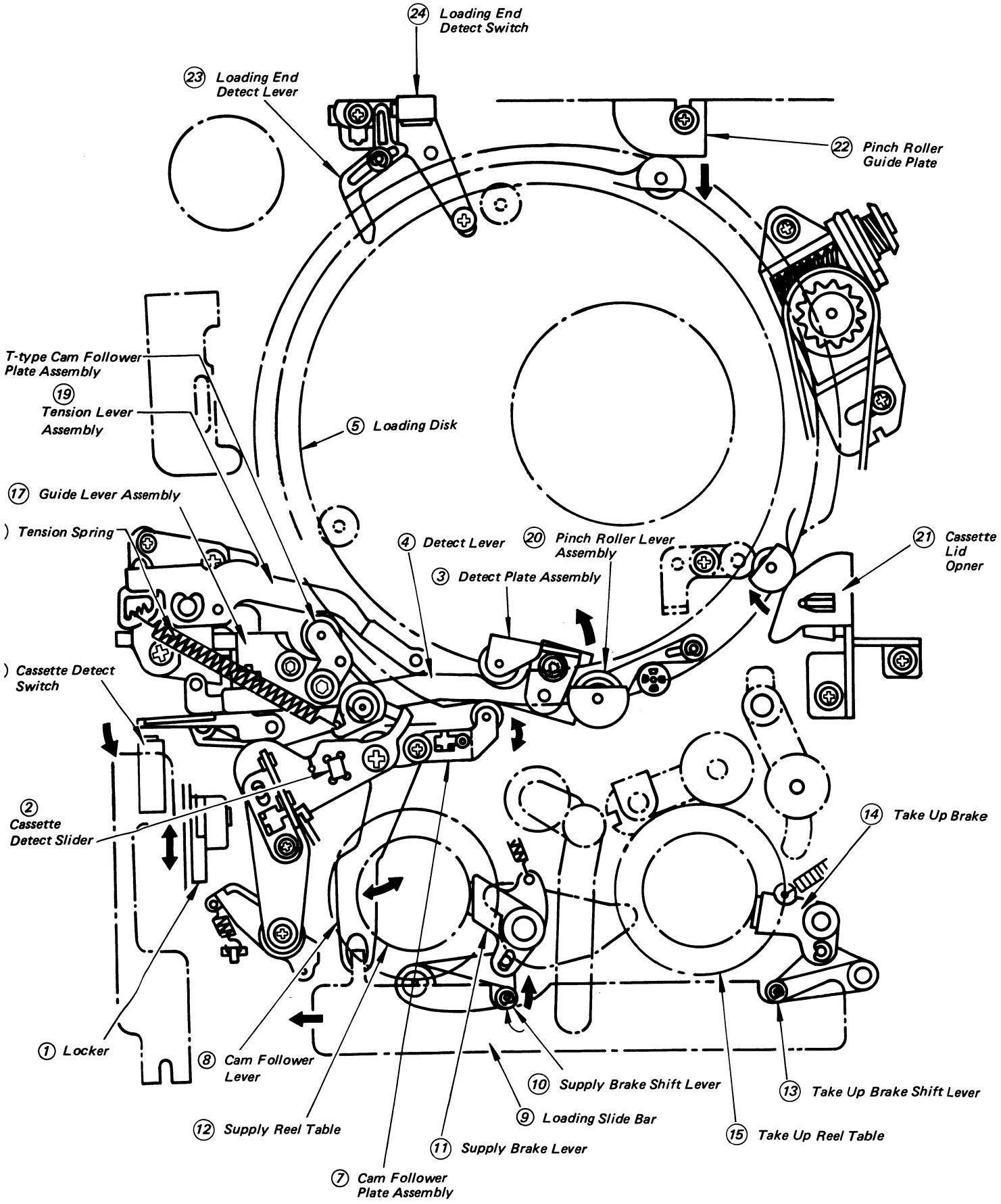



**Fig. 101. Tape Loading Arrangement**

## 7-2. Playback Operation and Tape Running (see Fig. 102)

The PLAY button is pressed.

- The play solenoid ① is energized to attract the solenoid lever ②. The play slider ③ is moved leftward (←) by the solenoid lever ②.
- The supply brake shift lever assembly ⑩ detaches the supply brake ⑪ from the supply reel table ⑤.
- The FF brake assembly ⑮ detaches from the supply reel table ⑤. The take up brake shift lever assembly ⑫ detaches the take up brake ⑬ from the take up reel table ⑥.
- The play sub-lever ⑨ turns around (↖).
- The play sub-lever ⑨ presses the play idler ⑧ to the take up reel table ⑥.
- The link ㉑ moves the shift lever ㉒ rightward (→).
- The tension lever assembly ⑳ moves up-leftward (↖) to carry the tape in a specified position.
- The band brake assembly ⑰ is pulled to contact with the supply reel table ⑤.

The cylinder ㉗ is revolved counterclockwise (↶).

- The reel belt (1) ㉘, the planetary gear unit ㉙ the reel belt (2) ㉚, the FF clutch assembly ㉛, the play belt ㉜, and the play pulley assembly ㉝ are moved one after another in this sequence to revolve the play idler ⑧ counterclockwise (↶).
- The take up reel table ⑥ is revolved clockwise (↘). The take up reel winds the tape.

The capstan motor revolves counterclockwise (↶).
The capstan belt revolves the capstan counterclockwise (↶).

- The pinch lock solenoid ㉔ is energized.
- The pinch lock plate ㉕ is turned clockwise (↷) to press the pinch roller to the capstan. (A tape is transported.)
- The slack lever ㉖ is turned clockwise (↷) to come into contact with the tape. The slack lever ㉖ checks the presence or absence of the tape and the amount of slack.

These operations are set the tape transport arrangement into the playback mode of operation. The tape is transported as shown in Fig. 110.

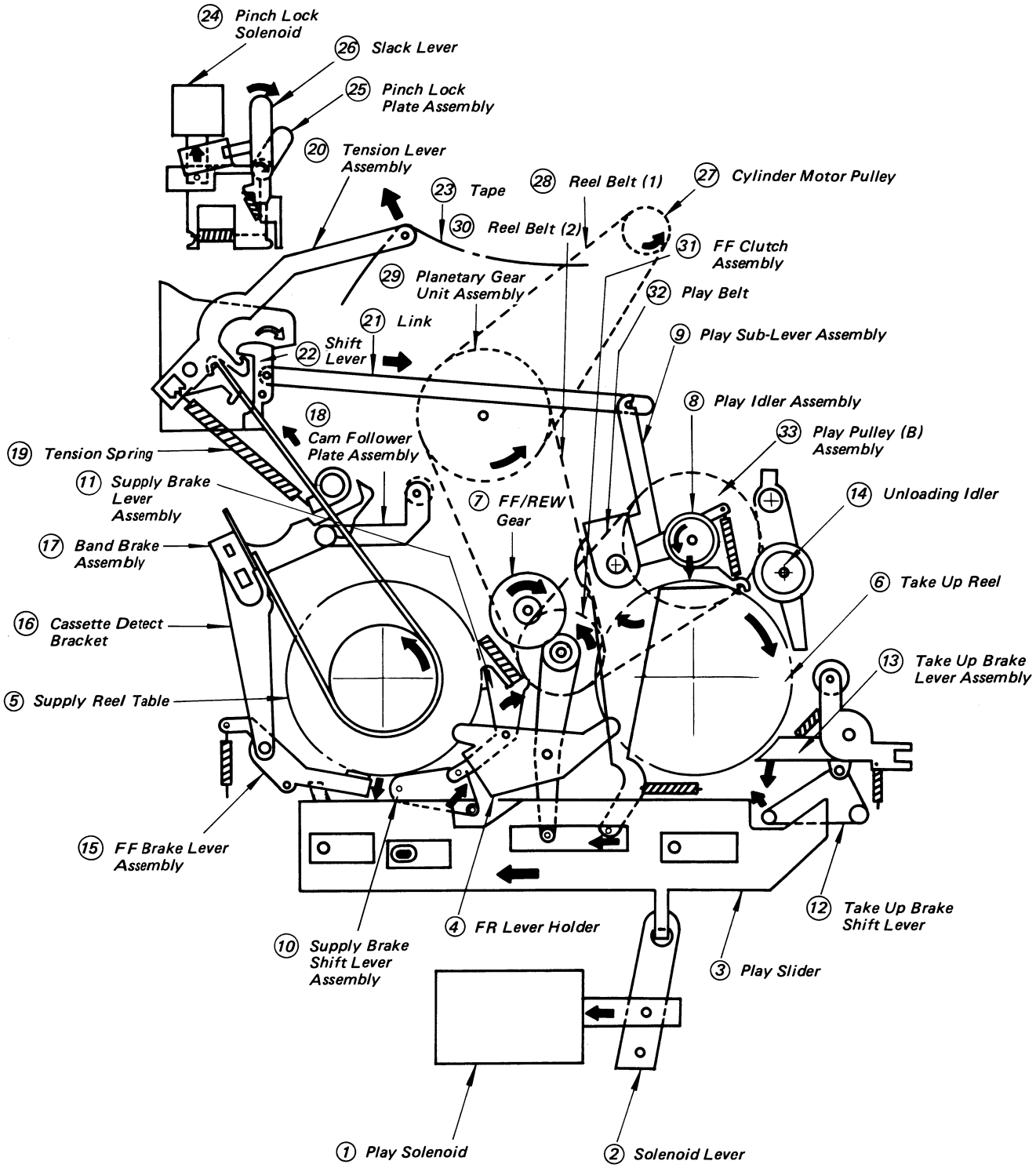



**Fig. 102. Playback, Recording, and Audio Dubbing Mechanics**

## 7-3. Recording or Audio Dubbing Operation and Tape Running (see Figs. 102, 103)

- The cassette compartment assembly is locked. (with cassette)
- The record safety plate ① is pressed downward (↓).
- The record safety switch ④ is reset.
- The tape is loaded (refer to Section 7-1 of the Tape Loading Operation.)

↓

The REC or AUDIO DUB button is pressed.

↓

The pause solenoid is energized.

↓

The pinch lock solenoid is energized and at the same time, the pause solenoid is deenergized.

**NOTE:** If the record safety tab on the cassette is broken, the record safety switch functions. Any of the REC and AUDIO DUB is not effective even if pressed.

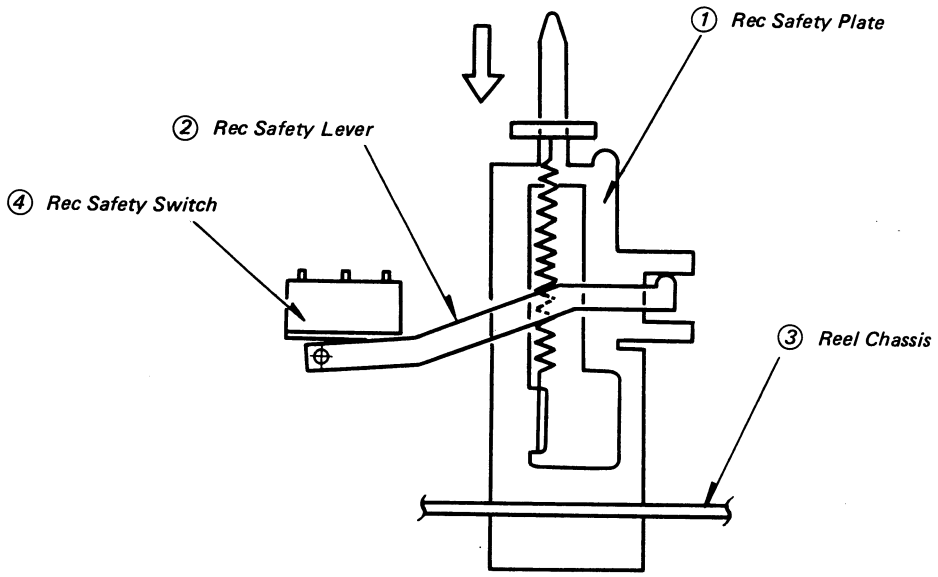



**Fig. 103. Record Safety Arrangement**

## 7-4. Fast-Forward Operation and Tape Running (see Fig. 104)

The FF button is pressed.

- The FF solenoid ① is energized.
- The solenoid lever ② moves the FF slider ③ to leftward (←).

The supply brake shift lever assembly ⑩ detaches the supply brake ⑪ from the supply reel table ⑤.

- The take up brake shift lever assembly ⑫ detaches the take up brake ⑬ from the take up reel table ⑥.
- The FR lever ⑦ is turned clockwise (↷) to engage the FF gear ⑨ with the take up reel table ⑥.

The capstan motor revolves counterclockwise (↶).

The capstan belt revolves counterclockwise (↶).

The cylinder is revolved counterclockwise (↶).

- The reel belt (1) ㉔, the planetary gear unit ㉑, and the reel belt (2) ⑳ are moved one after another to turn the FF clutch assembly ⑰ counterclockwise (↶).
- The FF gear ⑨ is revolved counterclockwise (↶).
- The take up reel table ⑥ is revolved clockwise (↷).

These operations are set the tape transport arrangement into the Fast-Forward mode of operation. The tape is carried as shown in Fig. 110.

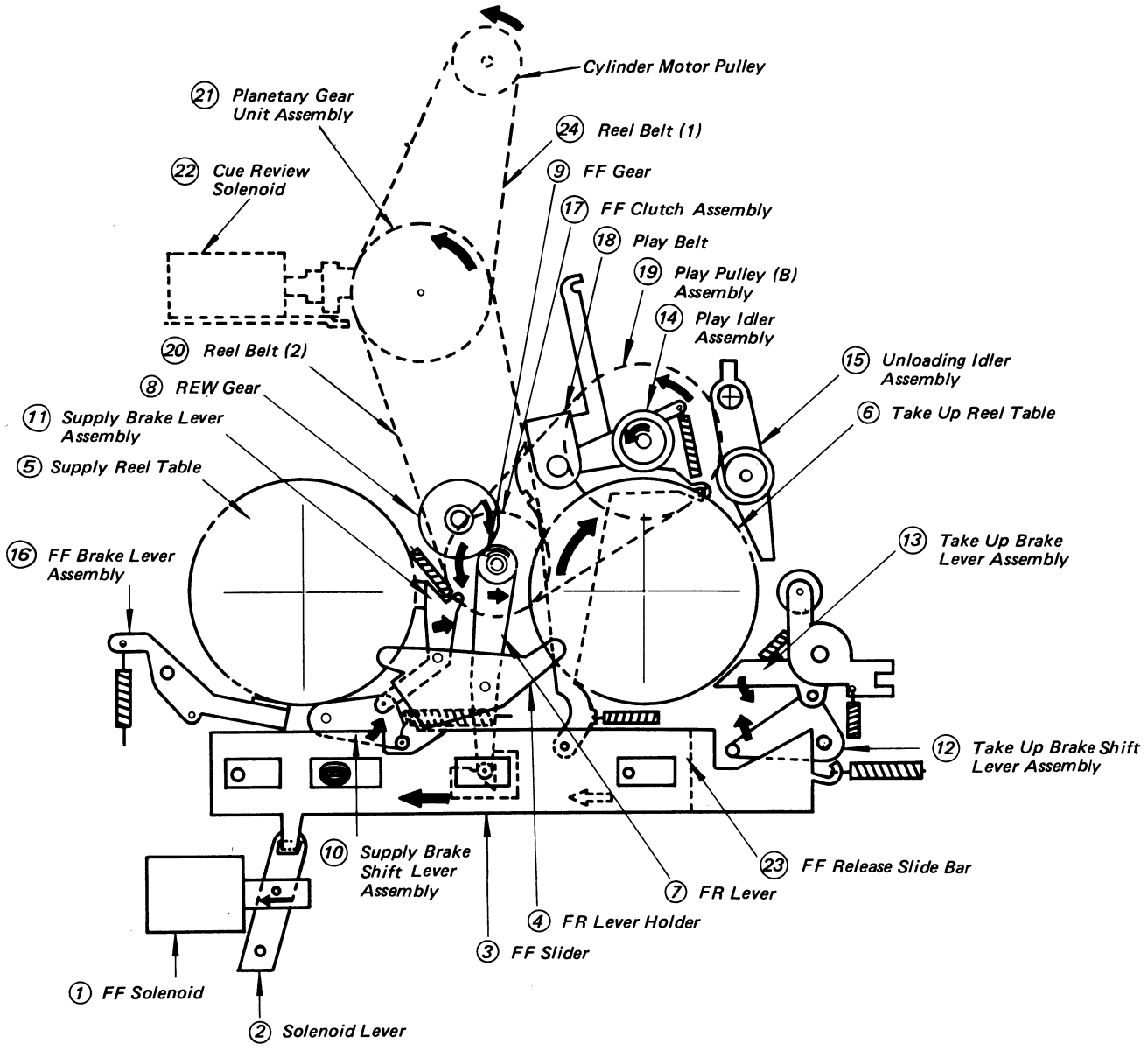



**Fig. 104. Fast-Forward Mechanism**

## 7-5. Rewinding Operation and Tape Running (see Fig. 105)

The REW button is pressed.

- The REW solenoid ① is energized.
- The solenoid lever ② moves the REW slider ③ to rightward (→).

The supply brake shift lever assembly ⑩ detaches the supply brake ⑪ from the supply reel table ⑤.

- The take up brake shift lever assembly ⑫ detaches the take up brake ⑬ from the take up reel table ⑥.
- The FR lever ⑦ is turned counterclockwise (↶) to engage the REW gear ⑧ with the supply reel table ⑤.
- The capstan motor revolves counterclockwise (↶).
- The capstan belt revolves the capstan counterclockwise (↶).
- The cylinder is revolved counterclockwise (↶).
- The reel belt (1) ㉔, the planetary gear unit ㉑, the reel belt (2) ⑳, the FF clutch assembly ⑰, and the FF gear ⑨ are moved one after another in this sequence to revolve the REW gear ⑧ clockwise (↷).
- The supply reel table ⑤ is revolved counterclockwise (↷).

These operations are set the tape transport arrangement into the rewinding mode of operation. The tape is carried as shown in Fig. 110.

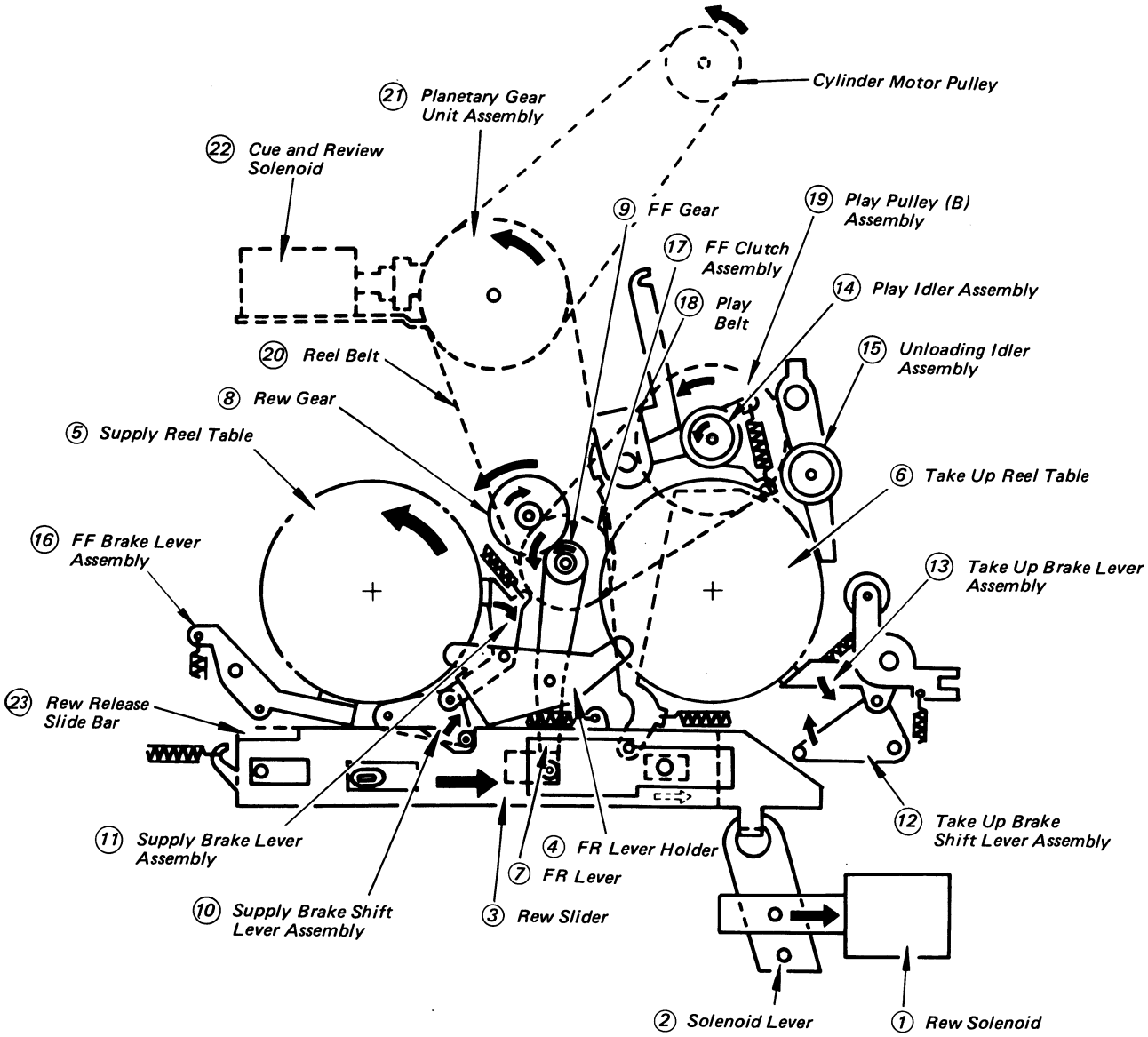



Fig. 105.

## 7-6. Picture Search Operation and Tape Running (see Figs. 106, 107)

### (a) Cue Mode

While pressing the CUE button.

The tape transport operates in the same way as in the Fast-Forward operation. (See Section 7-4. Tape speed is about 30 times the normal speed.)

The CUE button is released by the finger.

- The QR solenoid (22) is energized. The speed is reduced by the planetary gear unit (21). (Tape speed is about 10 times the normal speed.)
- Followed by the corresponding Fast-Forward operation steps given in Section 7-4.

These operations are set the tape transport arrangement into the cue mode of operation, which is different from the Fast-Forward mode in that the take up reel table rpm is slower.

**NOTE:** The planetary gear unit assembly is actuated by the Cue and Review only in the High Speed Cue mode.

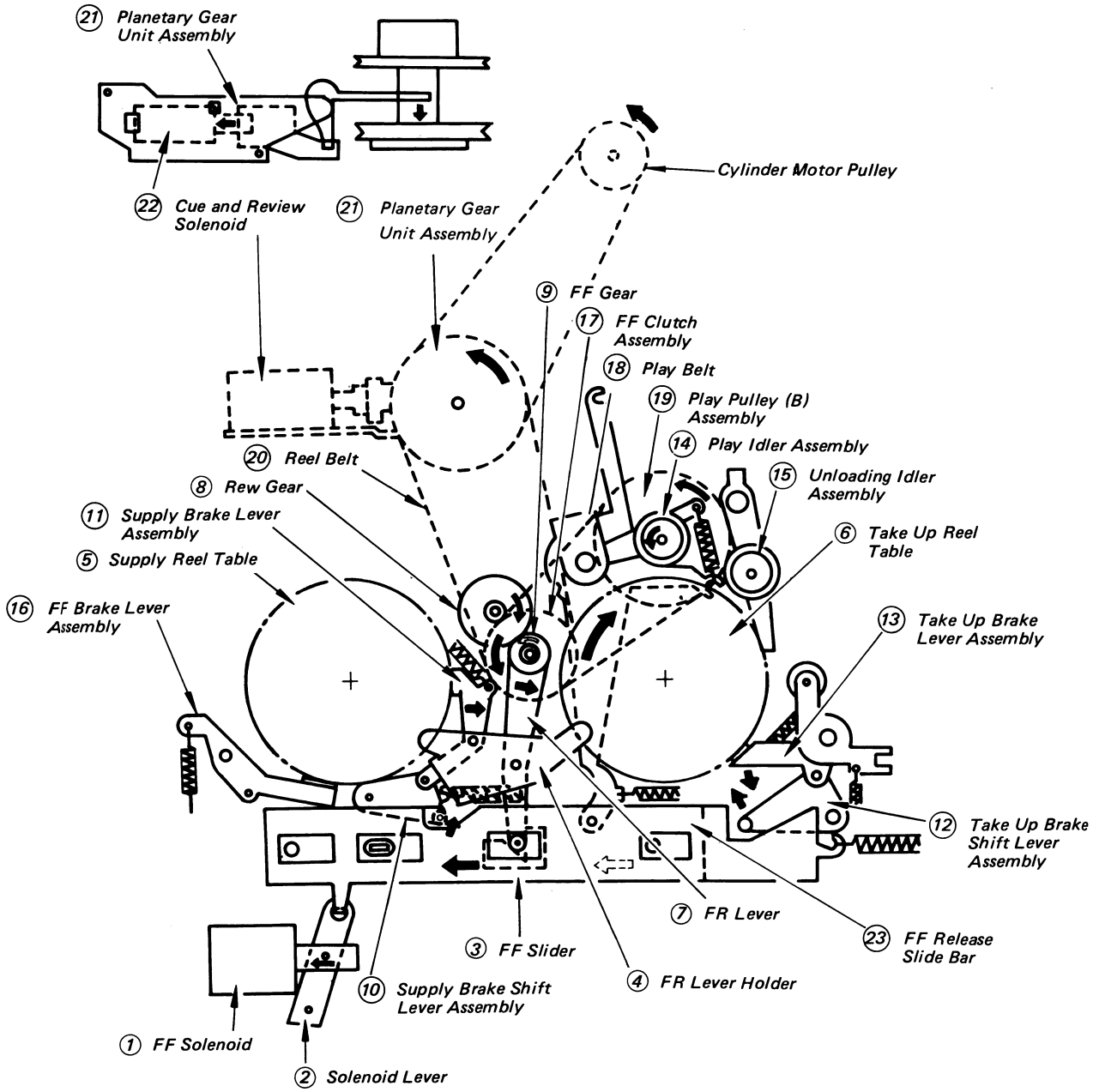



**Fig. 106. Cue Mechanism**

**(b) Review Mode**

While pressing the Review button.

The tape transport operates in the same way as in the rewinding operation.
(See Section 7-5. Tape speed is about 30 times the normal speed.)

The REVIEW button is released by the finger.

- The QR solenoid (22) is energized.
  The speed is reduced by the planetary gear unit (21). (Tape speed is about 10 times the normal speed.)
- Followed by the corresponding rewinding operation steps given in Section 7-5.

These operations are set the tape transport arrangement into the review mode of operation, which is different from the rewinding mode in that the supply reel table rpm is slower.

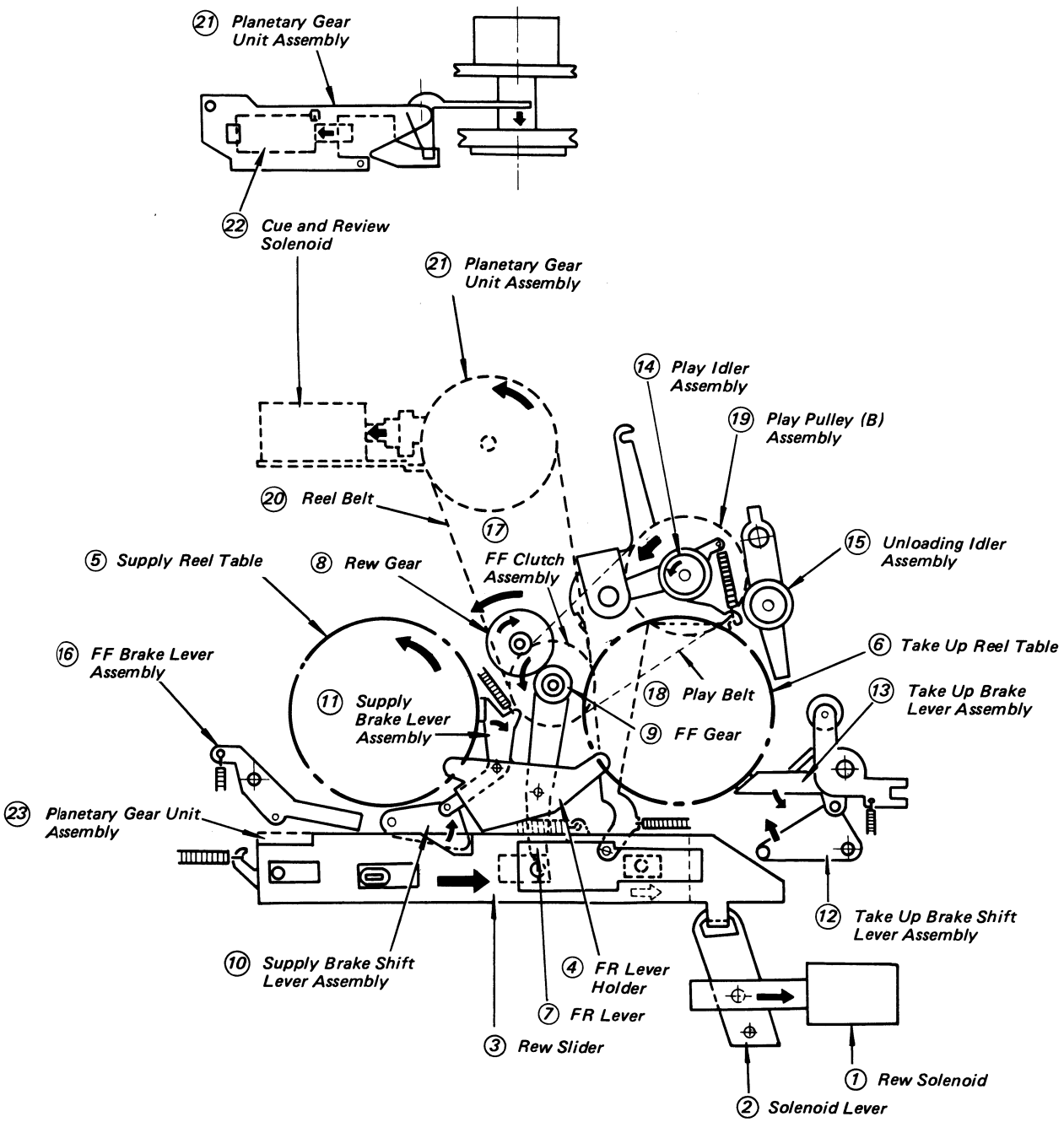



**Fig. 107. Review Mechanism**

## 7-7. Pause/Still Operations (see Fig. 108)

### (1) Still operation in playback mode (see Fig. 108)

The PAUSE/Still button is pressed.

- The capstan motor is stopped.
- The capstan stops, resulting in stop of the tape transportation.

These operations are set the tape transport arrangement into the still state in the playback mode of operation.

### (2) Pause operation in recording or audio dubbing mode (see Fig. 108)

The PAUSE/Still button is pressed.

- The pause solenoid (27) is energized.
- The pause lever assembly (28) is turned counter-clockwise (↖) to be pressed to the take up reel table (6) .
- The take up reel table (6) is stopped.
- The pinch lock solenoid (24) is deenergized.
- The pinch roller is detached form the capstan shaft.

These operations are set the tape transport arrangement into the pause state in the recording or audio dubbing mode of operation.

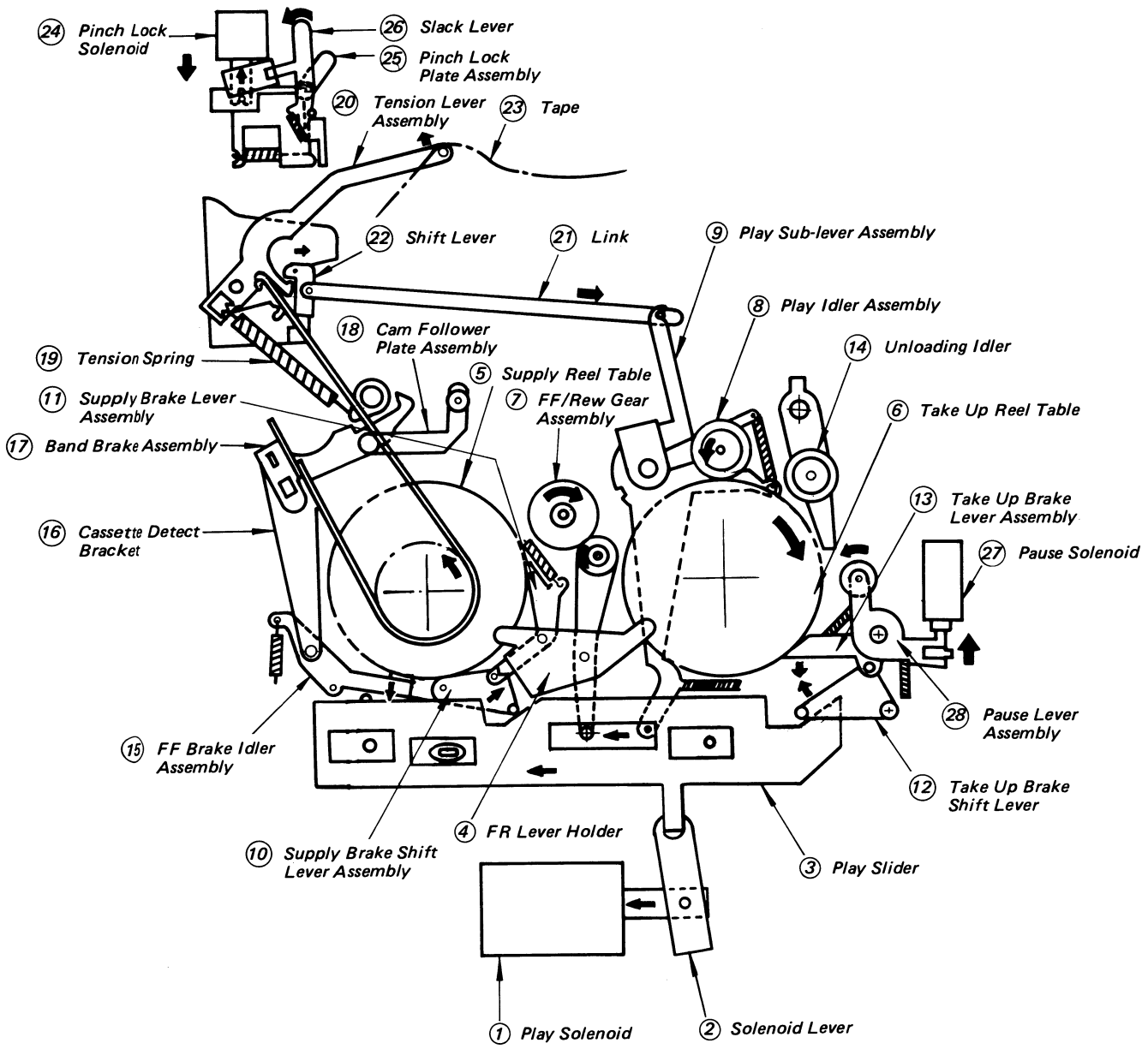



Fig. 108. Pause/Still Mechanism

## 7-8. Cassette Eject Operation and Tape Running (see Fig. 109)

**The EJECT button is pressed.**

- The eject solenoid ① is energized.
- The eject slide bar ② is moved leftward (←).
- The cam follower lever ③ is turned leftward (←), which causes the roller of the cam follower plate assembly ④ to unlock the loading disk ⑤ .
- The unlock lever ⑥ is turned and tends to lift the unlock slider ⑧ upward (↑) through the unlock spring ⑦ . The unlock slider ⑧ , however, can be moved a very little as the unlock spring ⑦ is extended because the roller of the detect plate assembly ⑨ is in contact with the inside of the disk. The cassette compartment assembly cannot be lifted up yet.
- The unloading sub-lever ⑩ is turned and the unloading spring ⑪ forces to press the unloading idler ⑫ to the take up reel table assembly ⑬ .
- The eject detect switch ⑭ is turned on.

**Tape unloading is started.**

- The roller of the cam follower plate assembly ④ rides upon the cam way of the outside of the disk to release the brakes from the supply and take up reel tables. The revolution of the gear of the loading drive assembly ⑮ is transmitted to the take up reel table ⑬ through the take up belt ⑯ . The tape ⑤ , then, is wound in as the disk is turned around.

**The loading disk is turned clockwise and is stopped by the stopper.**

- The detect plate assembly ⑨ comes into the cam way on the inside of the disk.
- The locker ⑰ is turned downward (↓) to lift up the cassette compartment assembly.

**The cassette detect slider is lifted up.**

- The roller of the cam follower plate assembly ④ is moved along the cam way on the outside of the disk and the both reel tables are braked.

**The cassetted detect switch ⑲ is turned off, which stops the loading motor, and in approximately 0.5 sec, the eject solenoid ① is deenergized. Tape unloading is completed.**

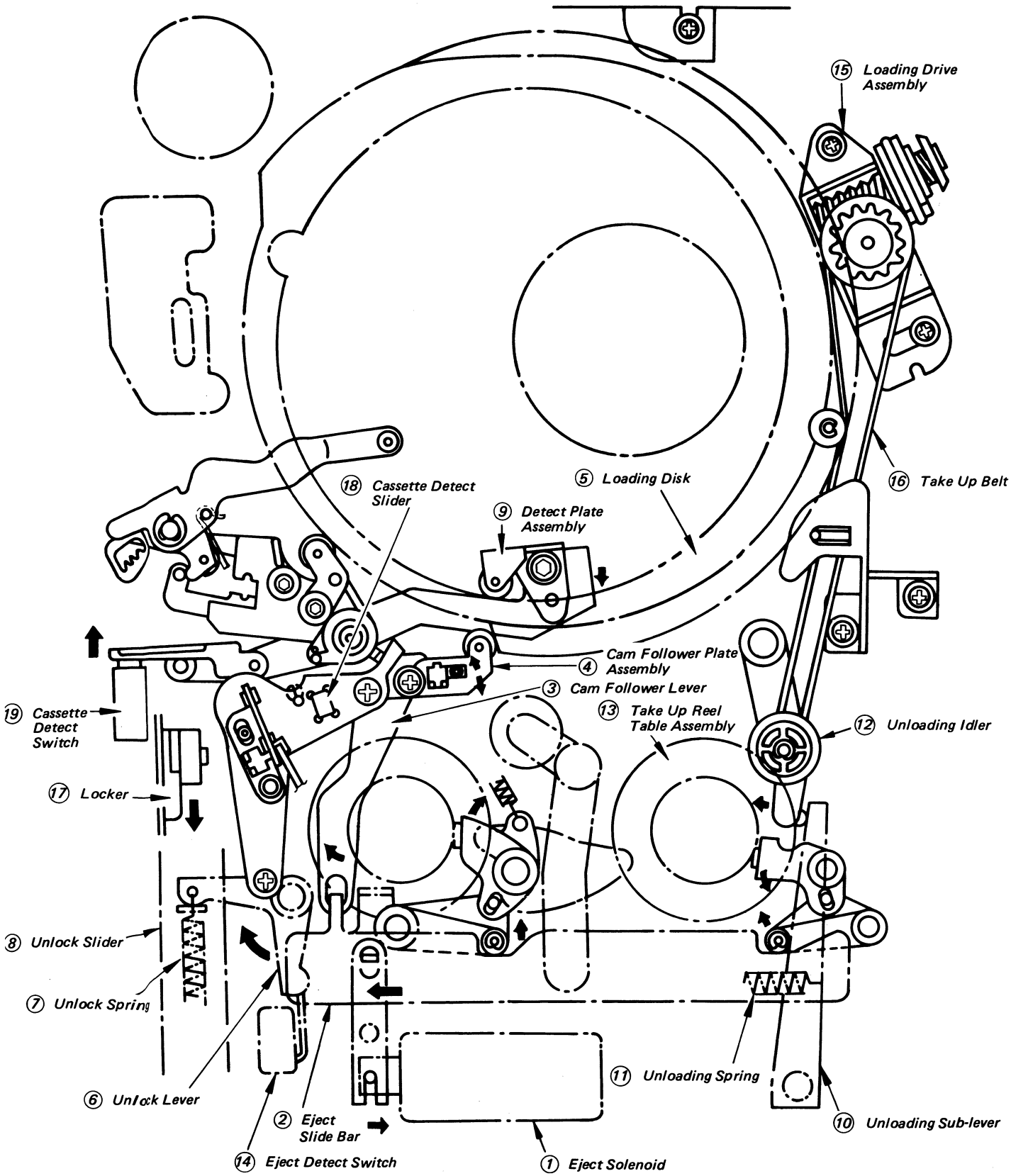



**Fig. 109. Cassette Ejecting Mechanism**

## 7-9. Stopping Operation from Fast-Forward, Rewinding, Cue, or Review Mode (see Fig. 102)

If the tape transport in either of the Fast-Forward, rewinding, cue, or review mode is stopped, the tape usually has a tension involved. This could cause the tape to stick to the cylinder. There is a device for avoiding such a sticking.

The STOP button is pressed in the course of the Fast-Forward, rewinding, cue, or review mode of operation.

The tape transport will be reset to the original condition.

The play solenoid ① is energized for a movement.

The tension lever ⑳ is turned counterclockwise (↶) to a specified point. (For the operation between the play solenoid ① and tension lever ⑳ , refer to Section 7-2, the "Playback operation and tape running".) The tape will be extracted a little.

The play solenoid ① is deenergized. The tension lever ⑳ , therefore, is returned to the stop position. This means that the amount of extracted tape is the slack needed.

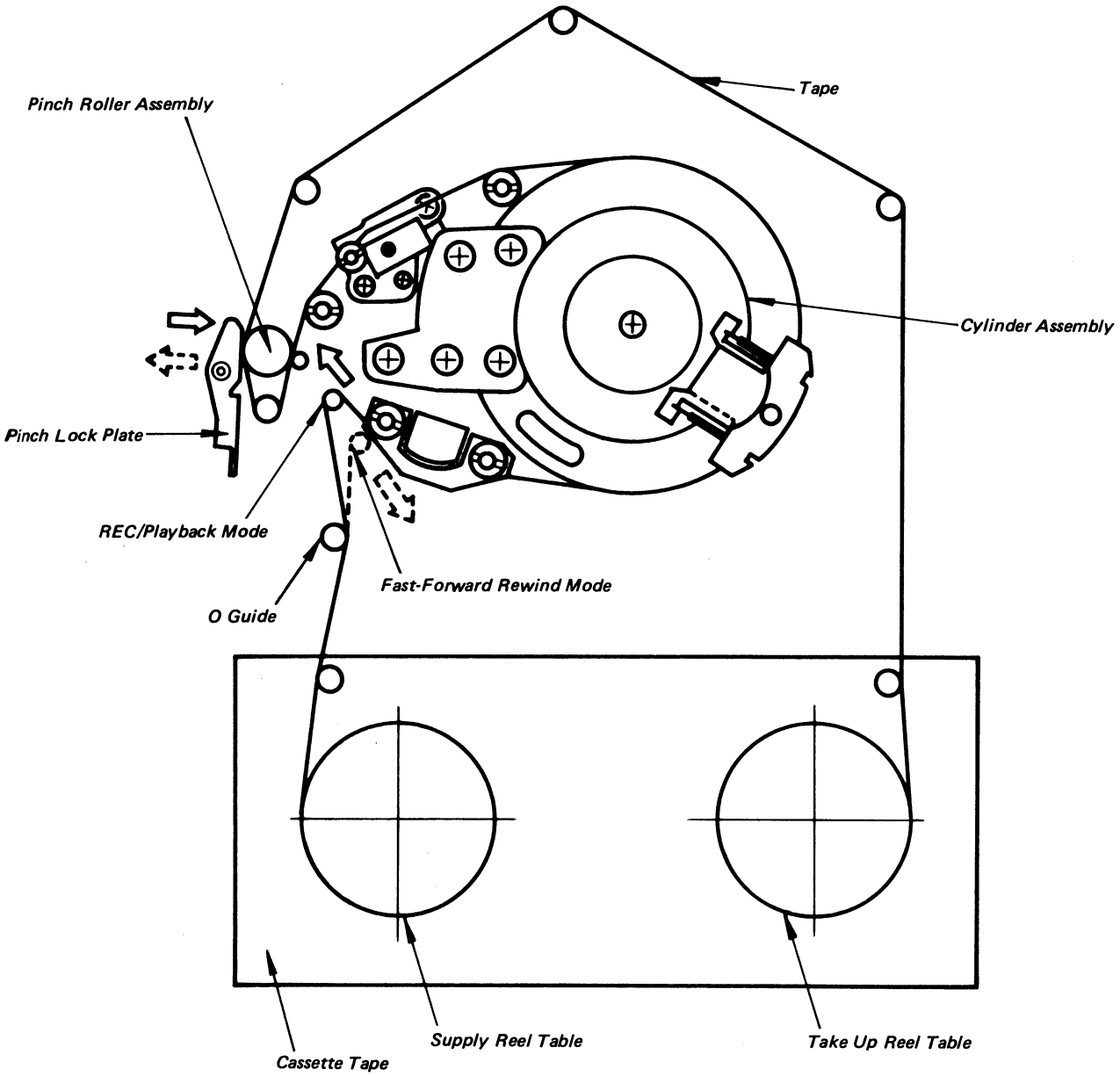



**Fig. 110. Tape Running Route on Tape Transport System**

# SECTION 3 MECHANICAL ADJUSTMENT

**8-1. Adjusting the Eccentricity Gauge in a Case Another Type.**

Proceed as below.

1. Set the cassette compartment the lift up state.
2. Unloosen the screw holding the cassette opner, place it cylinder side.
3. Install the eccentricity gauge on the light hand chassis ⑦. (see Fig. 111)
4. Adjust the height of gauge with the screw ②.
5. Tighten the screw ③.
6. Touch the probe ④ with the surface of the cylinder head assembly ⑤.
7. Turn the cylinder head assembly ⑤ counterclockwise (↶).
   Read the digit of gauge.
   Adjust the eccentricity of cylinder head assembly ⑤ in less than 2 μm.

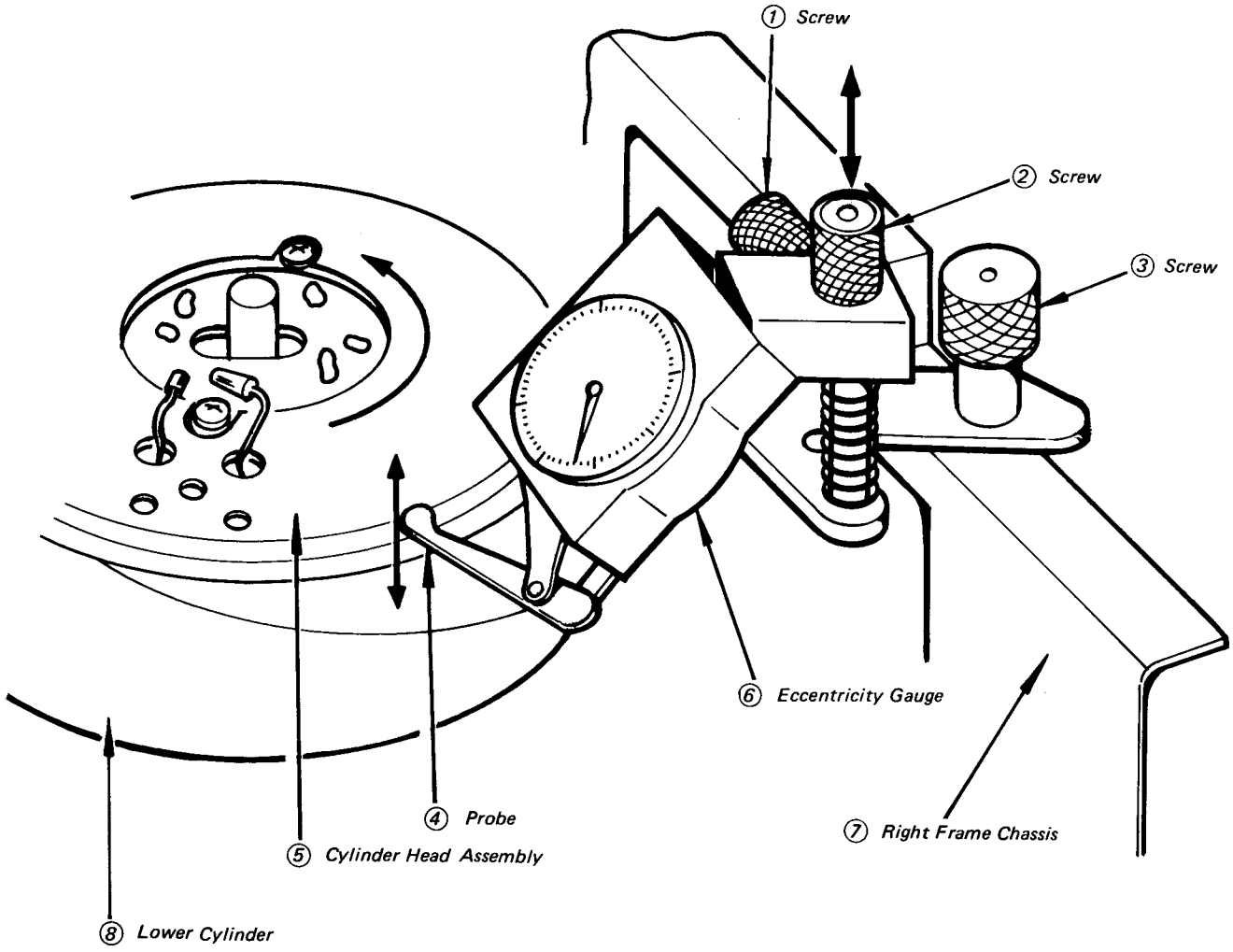



**Fig. 111. Eccentricity Gauge**